Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-8
Maintenance Manual

TC08

DECtape Controller

DEC-08-H3DA-D

PDP-8
TC08
DECTAPE CONTROLLER
MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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PREFACE

This manual has been written to explain the operation of the TC08 DECtape controller and to detail the fundamentals of its design. It is suitable for programmers familiar with the PDP-8 computer and practicing engineers experienced in digital systems. It assumes that the reader is familiar with the following publications:

TU55 DECtape 55 DEC-00-HZTA-D
PDP-8 User's Handbook
Logic Handbook C-105

The manual is divided into seven chapters.

Chapter 1 introduces DECtape, the TC08 Controller, and the TU55 and TU56 DECtape Transports.

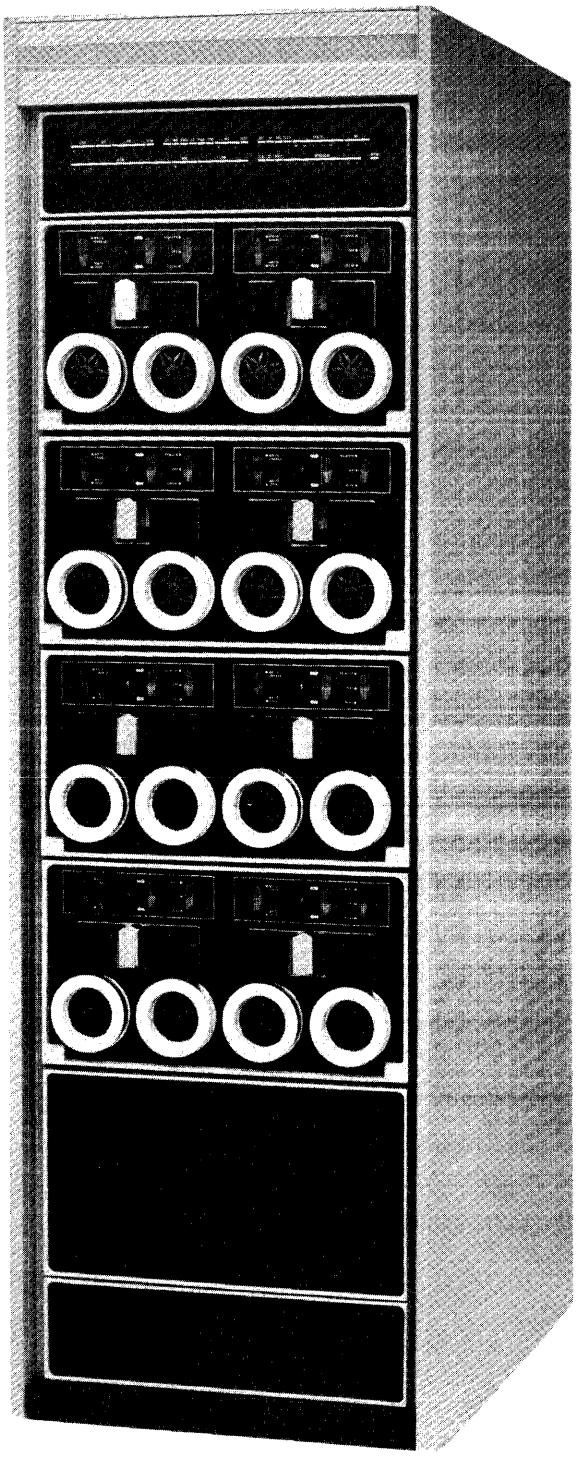
Chapter 2 covers the DECtape recording format, the system block diagram, and its instruction set. This chapter provides data required for a user or programmer.

Chapter 3 covers the basic architecture of the TC08. Detailed block diagrams, prints, and timing charts are presented with narrative.

Chapter 4 provides instructions for installing the TC08, and Chapter 5 outlines maintenance procedures.

Chapter 6 describes the DEC modules used in the TC08 but not explained in the Logic Handbook.

Chapter 7 contains the technical documentation for the TC08.



TC08 DECtape Controller

CHAPTER 1
INTRODUCTION

DECtape is a 10-track digital magnetic tape recording system designed and produced by Digital Equipment Corporation to store large amounts of digital information for computers. The system is divided into distinct units - a controller and number of transports. Each family of DEC computers uses its own DECtape controller to drive up to 8 DECtape transports. The PDP-8 family uses the TC08 or the TC08N controllers for its positive logic or negative logic PDP-8 computers, respectively. These controllers will operate either the TU55 or the TU56 tape transports (see Figures 1-1 and 1-2).

This manual explains the operation of the TC08 and TC08N controllers for the user, and details the fundamentals of their logic design as a guide to maintenance personnel.

1.1 THE TYPE TC08 AND TC08N CONTROLLERS

The TC08 and TC08N are the primary controls for up to 8 TU55 or 4 TU56 tape transports. These controls handle data and command signals for the PDP-8 family of computers through their I/O Bus or 3-cycle data break, and supply read/write circuitry, block format detection, and error detection logic to each transport. The TC08 is used with computers in the PDP-8 series which have positive logic I/O systems, and the TC08N is used with computers in the PDP-8 series which have negative logic I/O systems. The differences between the two controls are elementary; unless otherwise specified, any description of one applies to the other.

1.2 THE TU55 AND TU56 TRANSPORTS

Each transport contains motor, motor drivers, tape heads, and the logic necessary for selection, motion control, and data transfer.

The TU55 transport consists of one tape drive capable of handling 260-foot reels of 3/4-inch, 1-mil magnetic tape. The bits are recorded at a density of 350 ± 55 bits per track inch. The tape moves at a speed of 93 ± 12 inches per second; with 3 data tracks available, an effective information transfer rate of 350 x 93 x 3 = 97650 bits per second is achieved. Individual 12-bit words which are assembled by the TC08 control unit arrive at the computer approximately every 132 microseconds. The computer must accept this data in 20 microseconds. Data is stored in individually addressable blocks, which can be specified by the user and written into or read from in either direction of tape motion. Up to 190,000 12-bit words can be stored on a reel of tape.

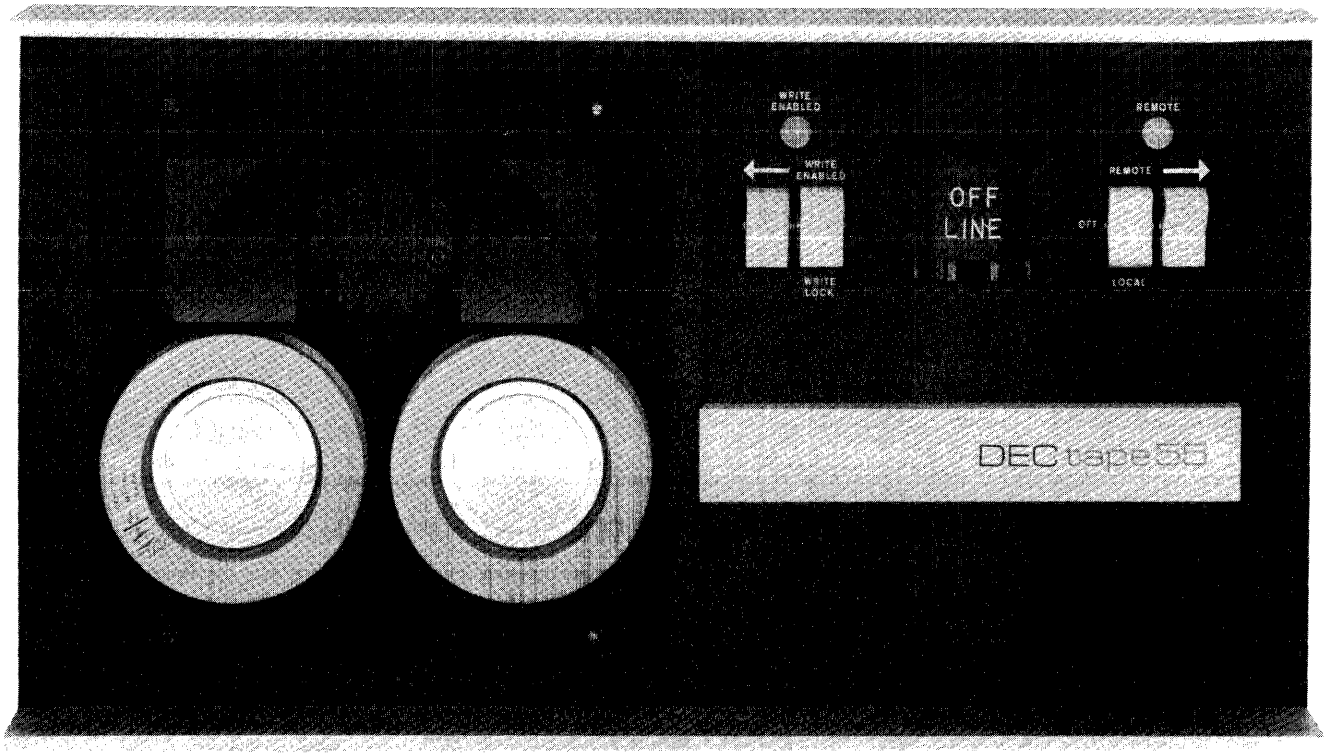


Figure 1-1 Type TU55 DECtape Transport

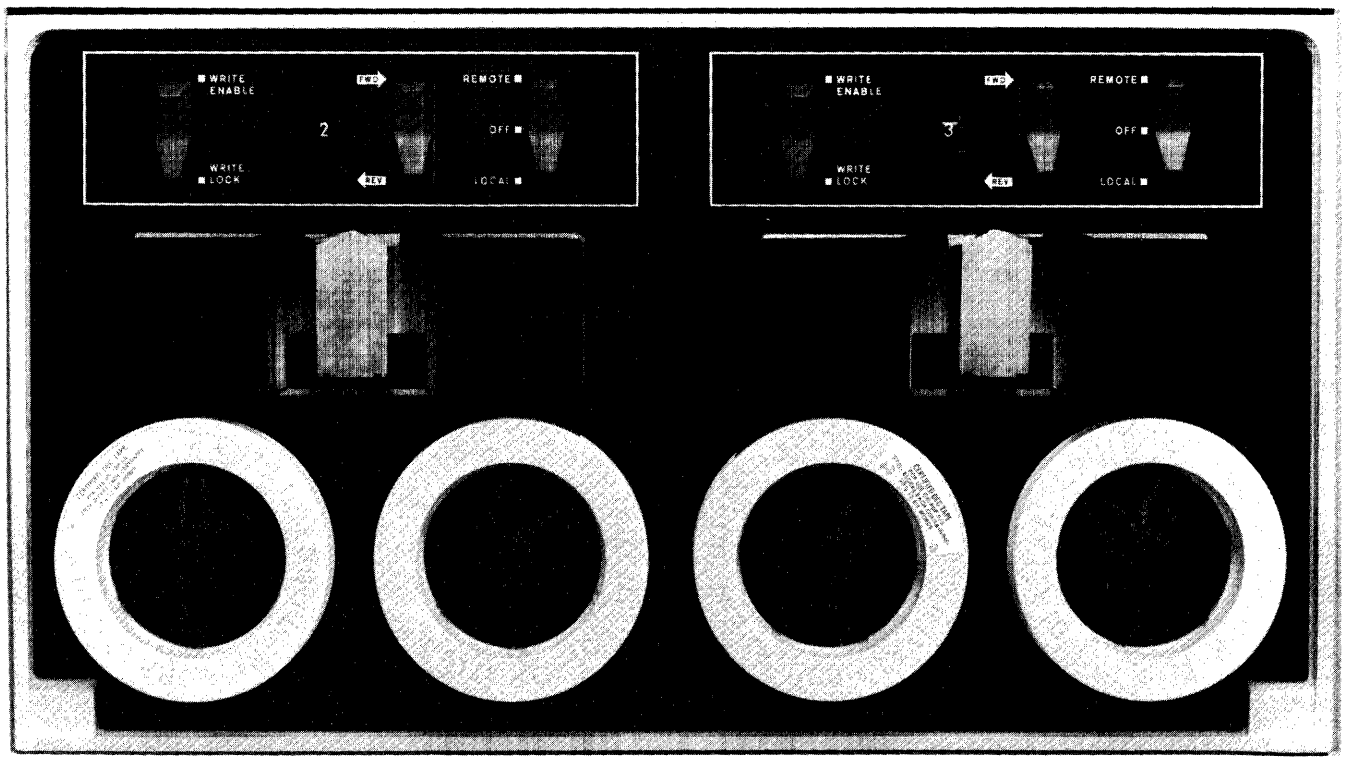


Figure 1-2 Type TU56 DECtape Transport

The TU56 transport consists of two identical tape drives, each like the TU55.

1.3 INSTALLATION AND ENVIRONMENTAL REQUIREMENTS

The TC08 controllers and both types of transports will mount in standard 19-inch cabinets. Cables from the PDP-8 I/O Bus and the three-cycle data break facility are connected to the controller, and two cables are chained from the controller through each transport to supply control and data information there. The system will operate in a temperature range of 60°F to 80°F at relative humidities of from 40% to 60%. These restrictions are due to the magnetic tape itself.

Chapter 4 describes installation procedures in detail.

CHAPTER 2
THEORY OF OPERATION

The purpose of Chapter 2 is to describe the operational nature of DECtape. It covers the recording format for data and control information, outlines and explains the system block diagram, and presents the instruction set used by the PDP-8 computer to control and communicate with the TC08 and the TU55 or TU56 transports.

2.1 DECTAPE RECORDING FORMAT

Two of the features of DECtape mentioned in Chapter 1, individually addressable blocks and bidirectional reading and writing, stem from the recording format used by DECtape. This format affects not only data, but also instructions telling DECtape what to do with the data.

Both the data and the instructions are stored in or read from the magnetic tape through read/write heads which magnetize the tape in one of two directions to represent a "0" or a "1", and read the same information back. There are ten such heads distributed along the width of the tape, each head covering a narrow path called a tape track or channel. Figure 2-1 shows a tape stretched over the ten heads to indicate how the width is divided into ten tracks.

The ten tracks and heads are divided functionally into five pairs. The two outside tracks are called timing channels. On these tracks signals are prerecorded at a fixed frequency, and used to strobe information into or from the other tracks. The tape controller synchronizes on these pulses. The two tracks next to the timing channels are called mark tracks. These record the instructions which tell the TC08 controller where the tape is and what type of data is stored in the associated information tracks. The information or data tracks are placed in the middle of the tape where the effect of skew is at a minimum. Like the timing and mark tracks, the data channels are paired up.

The reliability of this recording/reading system is high because the 10 tracks are divided into five pairs of counterparts. That is, corresponding heads for each track are wired in series and record and write the same information. During reading, the analog sum of the two heads is used to detect the correct value of the bit. Therefore a bit cannot be misread until the noise on the tape is sufficient to change the polarity of the sum of the signals being read. During writing, corresponding heads record the same information.

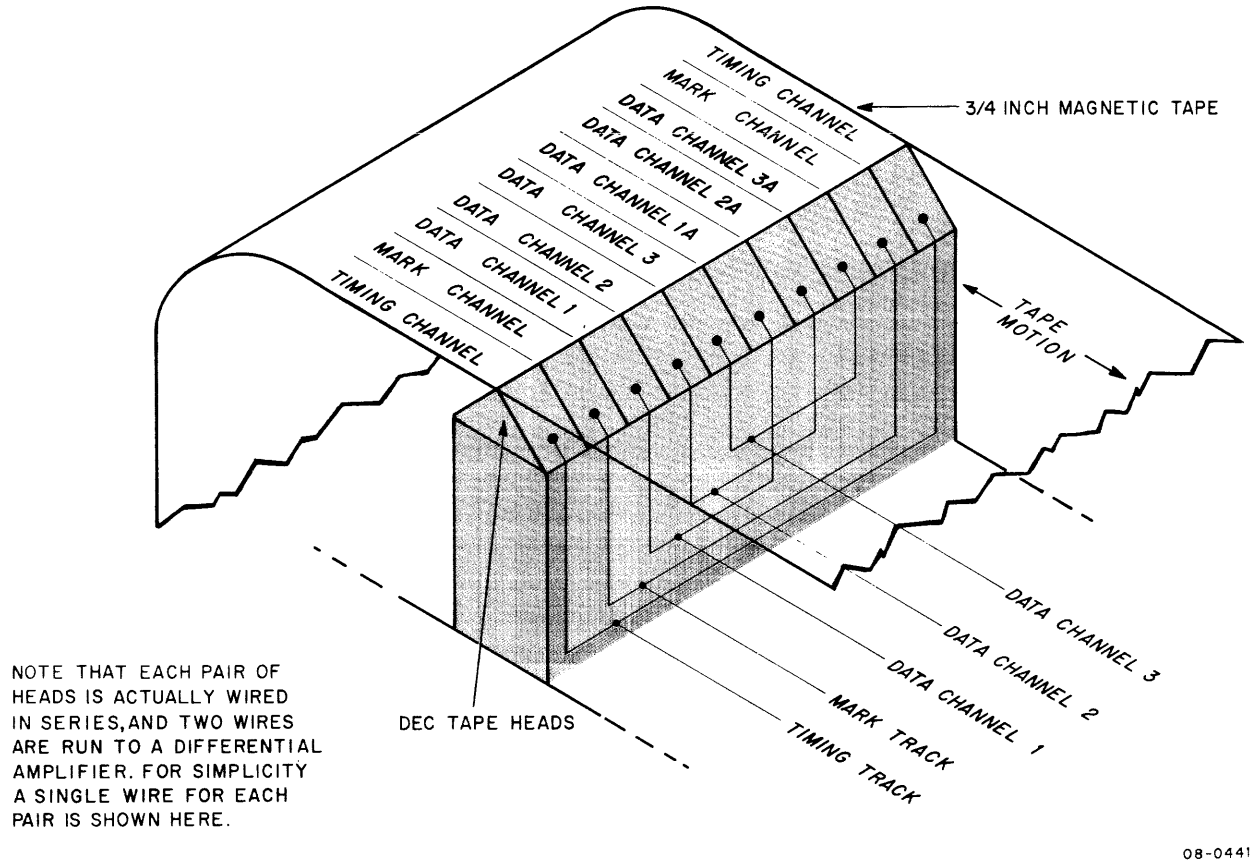


Figure 2-1 DECtape Heads and Tape Channels

In summary, the five pairs of tracks consist of the timing tracks used to strobe other tracks, the mark tracks which store instructions, and three data tracks. A 12-bit PDP-8 word, then, uses four slots of 3 data bits each.

2.2 DECTAPE DATA FORMAT

A 260-foot reel of DECtape, shown in Figure 2-2, is divided into three zones; two end zones and the recording zone. The end zones, about 10 feet long, are used to wind the tape around the heads and onto the take-up reel. They never contain data.

The recording zone is divided into blocks. Each block will store a specified number of data words and several control words. The number of data words a block will store is determined when the tape is preformatted with its timing and mark track. In standard format, 1474_{10} blocks, each with 129_{10} 12-bit words, can be stored on a 260-ft reel. The total length of the tape is equivalent to 884,736 data lines which can be divided into any number of blocks up to 4096.

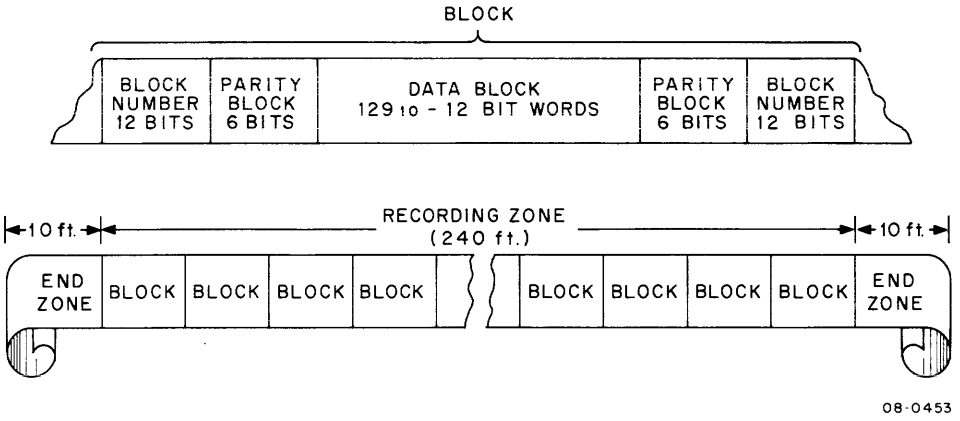


Figure 2-2 DECtape Data Blocks

Recording information on tape in blocks permits digital data to be partitioned into blocks of words which are interrelated and at the same time reduces the amount of storage area which would be needed to address individual words.

A simple example of such a partition is the coding of a program. A program can be stored and retrieved from magnetic tape in a single block format because it is not necessary to be able to retrieve only a subgroup of the coding. The computer usually wants the complete program, or none of it. It is necessary, however, to be able to identify and retrieve different programs, since they may not be related. They would be stored in different blocks of tape.

The data stored on a DECtape reel is organized into such blocks of data, with the following advantages:

a. Each block is numbered, and can be identified by the computer during a random search.
b. Errors can be detected within a block, using serial parity checking.
c. A block can be read or written while the tape is travelling in either direction.

A block is identified by a number recorded during tape formatting on the data tracks just before and after the area where data is stored in the block. This number is recorded at either end of a block so that it can be read from either direction.

Errors in reading or writing data are detected by calculating the parity of each data track as the block is written, and recording the checksum at the end of the block. When the block is read, the same parity checksum is calculated, and the result is compared with the original. If they compare favorably, the transfer is assumed to be valid. Otherwise, an error has occurred and the computer is notified. Since reading and writing must occur in either direction, the checksum must be recorded at each end of the block.

The average access time to any block is decreased if a block can be written or read from either direction. This is facilitated by writing the block number and leaving room for a parity checksum at either end of each block. However, there are further complications if a block is read in a direction opposite to the one from which it was written. The complications are covered in the next section.

The purpose of the pre-recorded mark track now becomes apparent. The code of this track identifies the information of the three data tracks as being a block number, a parity checksum, or data proper. In each case, the controller responds appropriately by either transferring the block number to the computer for identification, calculating the checksum, or transferring the data. The mark track must also perform several other functions, detecting such things as the end of tape zones, the beginning and end of blocks, and no operation (delaying) conditions. The various functions and their codes are summarized in Figure 2-3. Note that data is stored in cells which are 6 lines and 3 x 6 = 18 bits long. This will affect the acceptable length of a block, since it must be in increments of cells divisible by 12.

2.2.1 Block Lengths

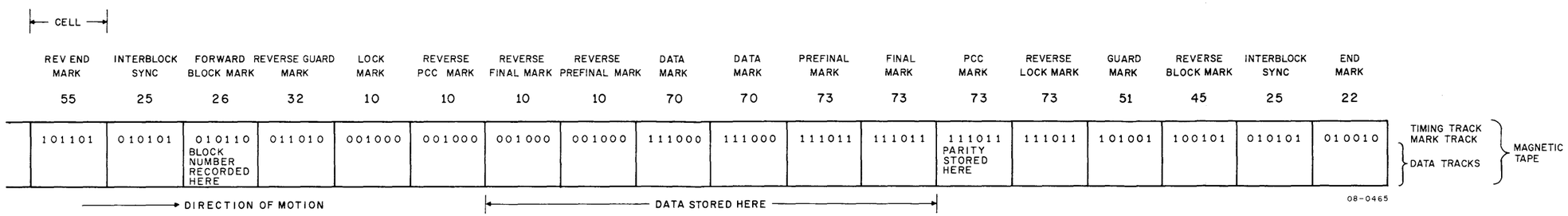
DEC provides a program called the DECtape formatter which is used to write the timing track, mark track, and block numbers onto a reel of DECtape. The formatter will allow the user to specify the number of data words he wants in each block within the constraints of a given formula. The formatter is described in TC08 DECtape Formatter, DEC-08-EUFA-D.

2.3 BIDIRECTIONAL READING AND WRITING

The freedom to read or write on DECtape in either direction raises some interesting problems. For example, if a bit is written as a 1 while the tape is travelling from left to right, then it would be read as such when the tape is travelling in the same direction during the read operation. Otherwise, that same bit is seen as a zero. Further, a complete word or mark track instruction read one way would be assembled in reverse order when read the other. Figure 2-4 illustrates this process. Here, a 42_8 read from left to right becomes a 56_8 if read in the reverse direction.

However, the problem is less complicated than it appears. 56_8 represents the obverse complement of 42_8; every number has one such counterpart, as shown in Table 2-1.

Data read into the computer in the opposite direction from that in which it was recorded is then in its obverse complement form. It can be reconverted by means of a simple algorithm. It is necessary only that the user be aware of how the data was recorded and read.



Code	Name	Function
55	REVERSE END MARK	This code identifies the end zone that the tape transport is leaving as it moves toward the data block zone. No action is taken by the controller.
25	INTERBLOCK SYNC	Code 25 is another no-op code which lies between blocks and for several feet on the inside of the end zones. It allows for turnaround time when reading the first and last block, and is used by the controller to synchronize its timing logic between blocks.
26	FORWARD BLOCK MARK	In this cell the number assigned the block by the formatter is stored. When the computer is searching for a block, it transfers this number into memory and examines it. When code 26 is decoded by the controller, it knows that the block number is ready and informs the computer.
32	REVERSE GUARD MARK	These two cells are no-op conditions which give the computer time to decide on what to do with the block it has identified.
10	LOCK MARK	
10	REVERSE PCC MARK	This is the last cell before a data cell. It is used to initiate the parity checksum logic. If the computer were writing, the first 12-bit word to be written is transferred to the controller during this cell, and every 4 lines thereafter.
10	REVERSE FINAL MARK	These two codes indicate the first and second data words respectively. Otherwise they have no special significance.
10	REVERSE PREFNAL MARK	
70	DATA MARK	The 70 code simply indicates that a data word is contained in the data tracks. The controller logic continually checks to see that the mark track is coded.
73	PREFINAL MARK	These codes indicate that the last two words of data are being transferred.
73	FINAL MARK	
73	PCC MARK	The parity checksum which was being calculated during the transfers is either deposited here during writing or compared during reading. If there is an error, the computer is notified at this point.
73	REVERSE LOCK MARK	These are no-op spaces which become useful when the tape is operating in the reverse direction.
51	GUARD MARK	
45	REVERSE BLOCK MARK	The block number is stored here to be picked up by the computer when the tape is traveling in the reverse direction.
25	INTERBLOCK SYNC	Has the same function as its counterpart at the beginning of the tape.
22	END MARK	When this code comes up, the program is informed that it has just run out of tape and that it had better do something about it! Note that it is the obverse complement of 55.

Figure 2-3 DECtape Data Format

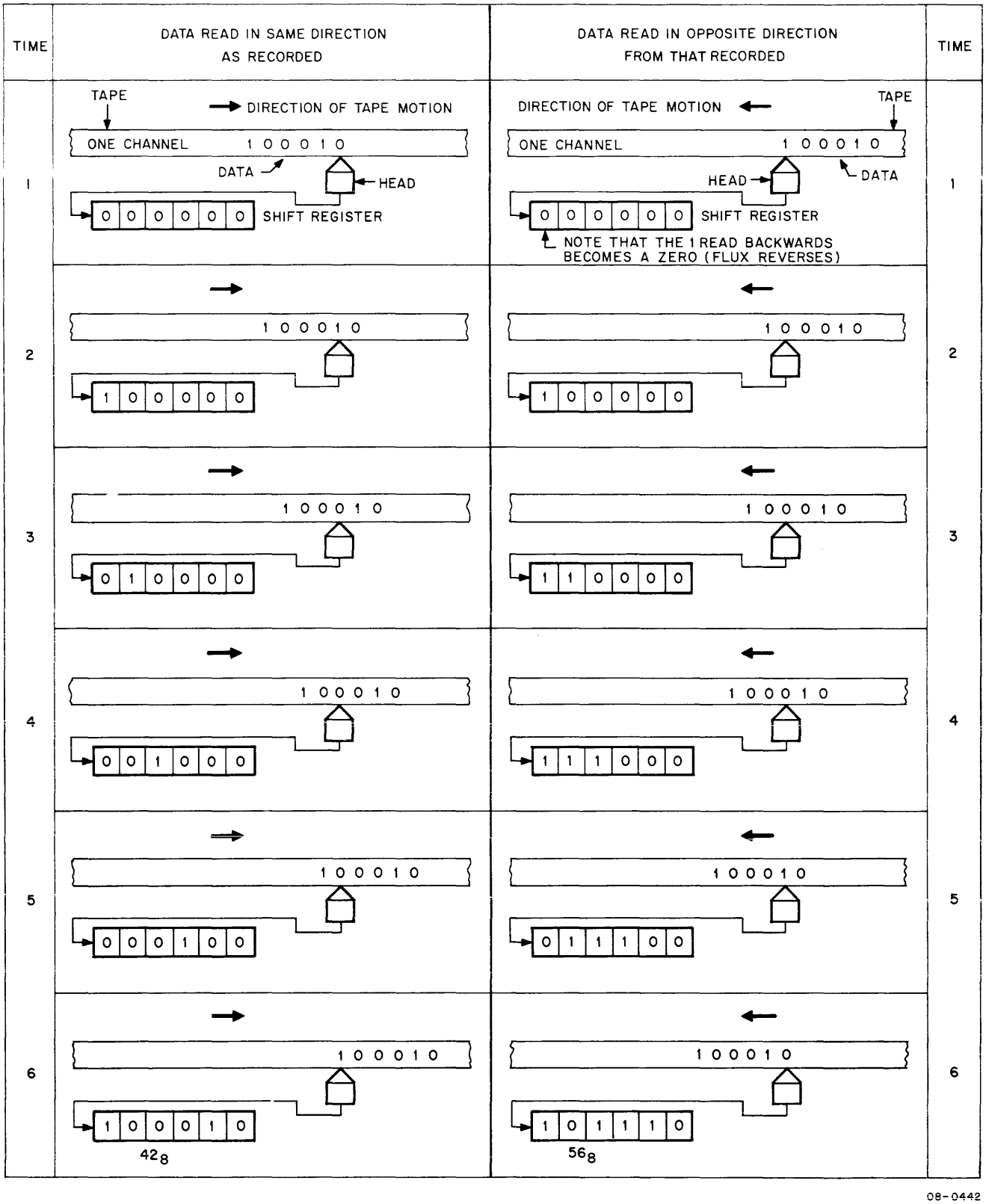


Figure 2-4 Bidirectional Reading and Writing

Table 2-1
Complements

Number (Octal)	Obverse Complement (Octal)
0	7
1	3
2	5
3	1
4	6
5	2
6	4
7	0

There is a problem with the information on the mark track, however; the mark track must identify data or control words no matter which way the tape travels, and these codes should read the same. Fortunately, some codes map into themselves as obverse complement. (For example, the obverse complement of 70 is 70 itself.) Such codes are used by the mark track to avoid the obverse problem. Note from Figure 2-3 that if the tape were travelling in the opposite direction, and all mark track codes were transferred to their obverse complement, the mark track read head would see exactly the same series of codes.

By using these principles, DECtape has been designed to be read or written in either direction, in randomly selected data blocks at high reliability. The programmer must be aware of how data was recorded in order to ensure that he has the data or its obverse complement; the TC08 controller handles all other problems.

A more detailed explanation of how DECtape actually records, and the nature of the instructions in the mark track will be covered in later chapters. This information is not needed to use DECtape.

2.4 THE TC08 BLOCK DIAGRAM

The TC08 is studied in two parts; the data transfer section and the control section, shown in Figures 2-5 and 2-6. Through the data transfer logic, the TC08 manipulates data in twelve-bit bytes between computer memory and its data buffer, using the three-cycle data break facility. Through the control section, the software operating system initializes the controller by selecting the transport with which it wishes to deal, the direction of tape motion of the transport, the function it is to perform, and the mode in which it will operate. The control also monitors the system for errors, and sets up interrupt flags to notify the computer when either an error has occurred or the function specified is finished.

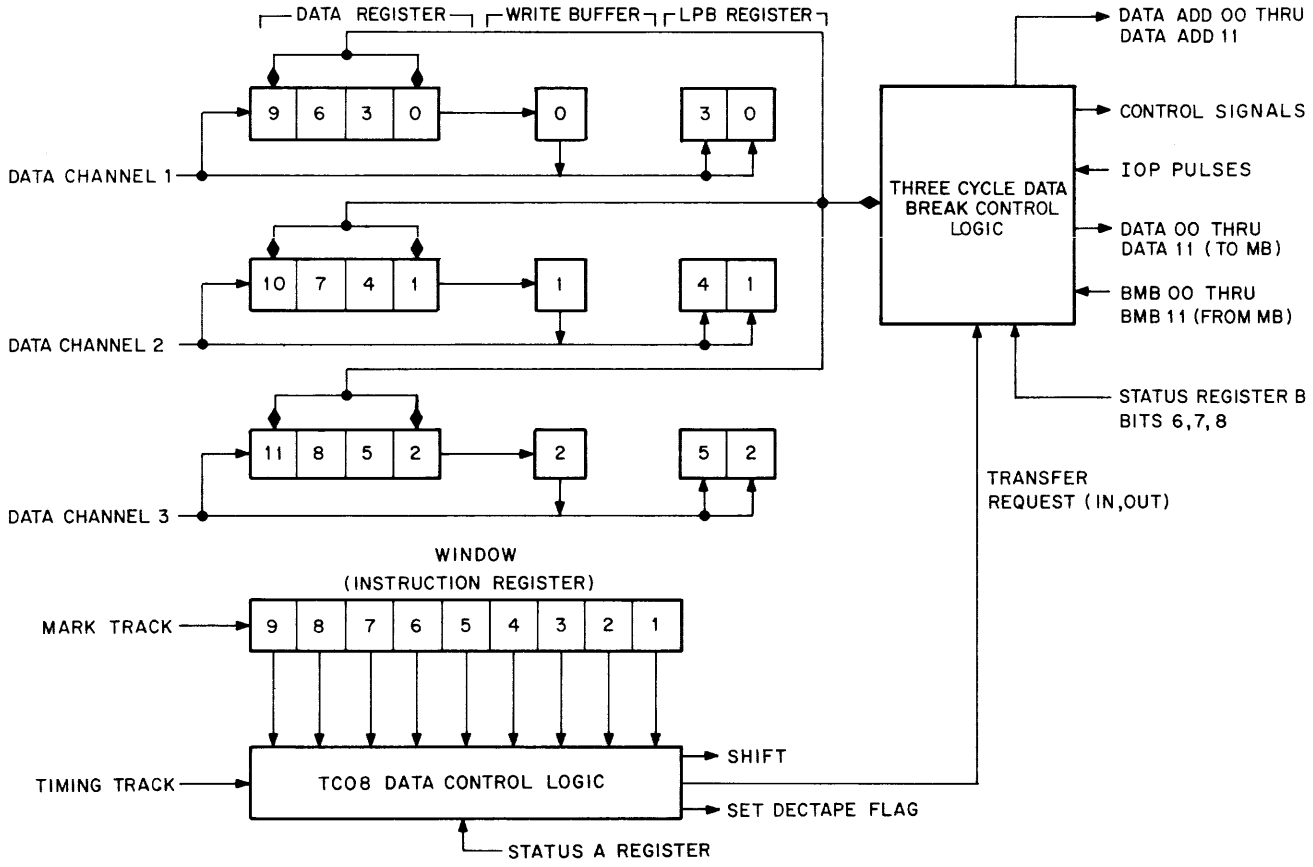


Figure 2-5 TC08 Data Transfer Section

2.4.1 The Data Transfer Section

The data transfer section is not directly available to the software operating system; once the controller has been initiated, the data section detects the position of the tape and carries out the specified operation. If the operation is to read data from the computer and store it on tape, then a three-cycle data break request is initiated and the correct block of words is transferred to the data buffer when the window register detects that block position on the tape. At the same time, the data section calculates the parity checksum in the longitudinal parity buffer, so that this sum can be checked at the end of the block.

If a write operation was specified, then the window register notifies the control when the first data word of the block is ready. This word is assembled into the data buffer; when the data buffer is full, the control requests that its contents be transferred to computer memory through the three-cycle data channel. Simultaneously, the parity checksum is calculated and deposited at the end of the block.

During a read operation, the computer must take the word in about 30 μs. During a write operation, the computer must supply a word in 16 μs.

STATUS REGISTER A BITS	FUNCTION
0-2	DECODED TO SELECT ONE OF EIGHT POSSIBLE TRANSPORTS
3-4	DETERMINES FORWARD, REVERSE STOP OR START MOTION
5	NORMAL OR CONTINUOUS MODE
6, 7, 8	DECODED TO SELECT ONE OF EIGHT POSSIBLE FUNCTIONS INCLUDING READ OR WRITE
9	ENABLES DECTAPE FLAG TO CAUSE PI WHEN SET
10	0-CLEARS ALL ERRORS FLAGS 1-NOTHING
11	0-CLEAR DECTAPE FLAG 1-NOTHING

STATUS REGISTER B BITS	FUNCTION
0	SET IF ANY ONE OF THE ERRORS DESCRIBED BY STATUS B BITS 1-5 OCCURS
1	MARK TRACK ERROR
2	END OF TAPE ERROR
3	SELECT ERROR
4	PARITY ERROR
5	TIMING ERROR
6, 7, 8	MEMORY FIELD SET FROM THE ACCUMULATOR
9, 10	NOT USED
11	DECTAPE FLAG SET AT THE COMPLETION OF A SELECTED FUNCTION

NOTE:

A BIT OF EACH STATUS REGISTER IS SET BY ITS CORRESPONDING BIT IN THE ACCUMULATOR WHEN THE PROPER LOAD STATUS IOT IS ISSUED. SIMILARLY, WHEN THE READ STATUS IOT IS ISSUED, EACH BIT OF THE STATUS REGISTER ADDRESSED IS READ INTO ITS CORRESPONDING ACCUMULATOR BIT.

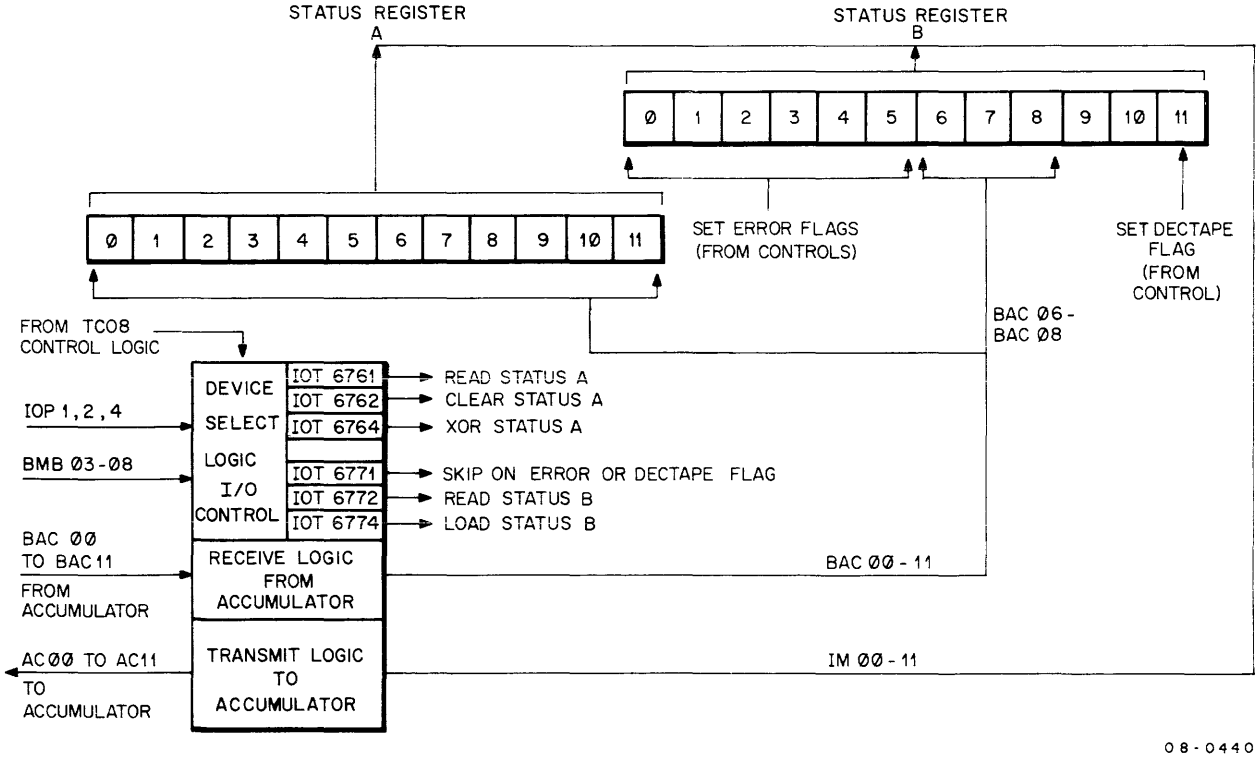


Figure 2-6 TC08 Control Section

These operations presumed that the software operating system had initiated its word count (location 7754) and current address (location 7755) to the block length and first address (minus one) to or from which the data was to be transferred.

2.4.2 The Control Section

The control section consists of two registers, status A and status B, and the device select logic. Status A register accepts commands, and status B reports the system status. The device select logic is used to clear, load, test, or read these registers under IOT control from the computer. Figure 2-6 summarizes the function of each bit in these registers, Table 2-2 expands on the figure, and Table 2-3 lists the IOT instructions and explains the use of each.

Table 2-2
Status A-bit Assignments

Function	Bit	Conditions
Transport Unit Select	0-2	Octal Code → Unit 000 → 8 or 0 001 → 1 010 → 2 011 → 3 100 → 4 101 → 5 110 → 6 111 → 7
Motion	3	0 = Forward (FWD) 1 = Reverse (REV)
	4	0 = Stop motion (STOP) 1 = Start motion (GO)
Mode	5	0 = Normal mode (NM) 1 = Continuous mode (CM)
Function	6,7,8	Code → Operation 000 → Move 001 → Search 010 → Read data 011 → Read all 100 → Write data 101 → Write all 110 → Write timing 111 → Unused (causes select error)
Enable the Interrupt	9	1 = Enable DECtape control flag (DTCF) to the program interrupt
Error flag	10	0 = Clear all error flags 1 = Error flags undisturbed
DECtape flag	11	0 = Clear DECtape flag 1 = DECtape flag undisturbed

Table 2-3
DECtape Instructions

Mnemonic	Octal Code	Operation
DTRA (read status register A)	6761	The contents of status register A are loaded into the accumulator by an OR transfer.
DTCA (clear status register A)	6762	Status register A is cleared. The DECtape and error flags are undisturbed.
DTXA (load status register A)	6764	Bits 0 - 9 of the status register are complemented if their corresponding bits in the accumulator are set to a 1. In other words, the exclusive OR between corresponding bits is loaded into the status A register, and bits 10 and 11 of the accumulator are sampled to control the clearing of the error and DECtape flags, respectively. Loading status register A from AC 0 through 9 establishes the transport unit select, motion control, and function, and enables or disables the DECtape control flag to request a program interrupt as described in DTRA. The accumulator is cleared.
DTSF (skip on flags)	6771	The contents of both the error and DECtape flags are sampled. If any flag is set, the contents of the program counter are incremented by one to skip the next sequential instruction.
DTRB (read status register B)	6772	The contents of status register B are loaded into the accumulator by an inclusive OR transfer. The bit assignments are as follows. AC0 = Error flag (EF) AC1 = Mark track error (MK TRK) AC2 = End-of-tape error (END) AC3 = Select error (SE) AC4 = Parity error (PE) AC5 = Timing error (TIM) AC6-8 = Memory field (MF) AC9-10 = Not used AC11 = DECtape flag (DTF)
DTLB (load memory field of status register B)	6774	The memory field portion of the status B register is loaded from accumulator bits 6-8. The accumulator is cleared, and the error flags are left undisturbed.

2.5 FUNCTIONS AND FLAGS OF THE CONTROL SECTION

Although the instruction set of the DECtape system is simple, the effects of these instructions are not. In this section, each of the functions that the TC08 will perform and the possible results of the operation are described in detail.

2.5.1 Functions of the Status A Register

2.5.1.1 Transport Unit Select - Each unit can be dialed into a particular selection address by means of a switch on the front of the transport. When the octal code matches the selection address, only that transport responds to the TC08 controller.

2.5.1.2 The Motions - GO asserted by loading a 1 into bit 4 allows the selected transport to move either forward (clockwise) or reverse, according to the contents of bit 3. If STOP is selected, then the machine does not move in any direction, or ceases to rotate in the direction it is moving. It should be noted that each transport remembers the motion it is selected to perform, and if the TC08 controller selects another transport without stopping the first, then the transport's memory keeps it moving. The functions are not performed when this transport is not selected, however.

2.5.1.3 The Modes - Associated with each of the functions are two modes, called normal and continuous. The difference in response for each mode varies with the functions, as explained in the following paragraphs.

2.5.1.4 The Functions -

a. Move - The move function is used to rewind tape. Code 000 of bits 6, 7, and 8 initiates tape motion in the selected direction, provided GO is also on. The mark track is read, but only the end of tape instruction is decoded. End of tape posts an error flag and causes an interrupt to the PDP-8. If the tape control is unselected but not stopped, it continues to run; however, the end of tape is not detected. The state of mode is irrelevant.

b. Search - The search function is used to search for blocks. When a block number is detected by the mark track, the three-cycle data break control transfers the number into the address specified by the current address register. The current address register is not incremented, so that successive block numbers always go to the same address. The word count register is incremented, however, as each block number is passed. If the mode is set to normal, the DECtape flag is set each time a block number is detected. This causes an interrupt, and the program can identify the block number. In continuous mode, no interrupt occurs until the word count register overflows. This search operation is most efficient when both modes are used in the following way:

(1) The current block number is detected in normal mode.

(2) The difference between it and the desired block number is computed, and the direction corrected, if necessary.

(3) The two's complement of the difference is loaded into the word count register.

(4) The TC08 is changed to continuous mode.

(5) On the next interrupt, the transport is over the desired block. The block number is in the address specified by the current address register.

2.5.1.5 Read Data - This function reads data in either direction and transfers blocks of data into core memory, with the transfer controlled by tape format. In the normal mode, DTF is set at the end of each block, causing a program interrupt. In the continuous mode, transfer stops and the DTF is set when the word count overflows; however, the remainder of the block in which the overflow occurred is read for parity checking, after which the DTF is set.

2.5.1.6 Read All - This function allows the reading of all data bits on tape after the tape motion attains speed. The three information tracks are continuously read and transferred to the computer. The mark track is used only to check for mark track and end of tape errors. During the normal mode, the DECtape flag is set at each data transfer. During continuous mode, the DECtape flag is set only when a word count overflow occurs.

2.5.1.7 Write Data - This function is used to write blocks of data in either direction, with the transfer controlled by the standard tape format. When a word count overflow occurs during the writing of a block of data, zeros are written in all the remaining lines of tape until the end of a block; the checksum over the entire block is then written. The DTF is set in a manner similar to that for the Read Data function.

2.5.1.8 Write All - This function allows the writing of all bits on tape even though the information is not in the standard tape format. The mark track is used only to check for mark track and end of tape errors. The DTF is set for the same conditions described for Read All. This mode is used to write block numbers on tape.

2.5.1.9 Write Timing and Mark Tracks - When the controller is put into this mode, it is ready to format a DECtape reel by adding the timing marks and the mark track. In normal mode, the DECtape flag is posted after each word is transferred to the mark track (every four lines); in continuous mode it is posted as soon as the word count overflows. A complete description of the program is given in the TOG-8 DECtape formatter description, available from the DEC program library.

2.5.1.10 - Enable to Interrupt - The TC08 control has an Enable-to-Interrupt (ENI) function which permits the program to remove the TC08 from the program interrupt of the PDP-8 processor. This bit activates it.

2.5.2 Errors and Flags of the Status B Register

This register contains 6 bits of error status information, 3 memory field bits, and the DECtape flag bit. Their functions are explained in the following paragraphs.

2.5.2.1 Error Flag - Bit 0 - This flag is set if any one of the five following error flags come up. These conditions stop transport motion, except for the parity error (bit 4), and all of them cause a program interrupt if the facility is enabled.

2.5.2.2 Mark Track Error - Bit 1 - The output from the mark track instruction register is tested every time an instruction should appear. If one does not, this indicates that the mark track is not recorded properly, and that an error has occurred. Bit 1 and, therefore, bit 0 are posted.

2.5.2.3 End of Tape Error - If the instruction register of the mark track decodes an end zone indicator, then bit 2 is set and, therefore, bit 0. A subsequent program interrupt stimulates the computer to find out what happened.

2.5.2.4 Select Error - This flag examines and compares various switches and status A functions, and will detect four incongruous combinations. These are:

a. When the transport unit select code loaded into the status A register specifies either more than one transport or none at all. This occurs when two selected transports are set to the same number, or none is set to the correct code.

b. When a write function is specified while the WRITE ENABLE/WRITE LOCK switch on the selected transport is set to the WRITE LOCK position, which inhibits writing.

c. When bits 111 are set into the function bits 6, 7, and 8 of status A, indicating a nonexistent function.

d. When the WRTM/NORMAL switch and the function selected do not coincide (e.g., trying to format on NORMAL).

2.5.2.5 Parity Error - This error occurs if the longitudinal parity buffer shows an error at the end of a block during a read data function. In normal mode, the error flag is set when the DECtape flag is set.

2.5.2.6 Timing Error - This flag monitors possible timing errors, which are:

a. If the data break request is not answered in 30 μs, some of the data is lost.

b. If the DECtape flag is not cleared by the program before the control attempts to set it again, the condition which set it was not serviced, and was probably lost.

c. If the read data or write data function is loaded into the status A register while the read heads are over a data section of the block, the complete block can not be transferred, and an error condition is present.

2.5.2.7 The Memory Field - This three-bit register is set by the computer to specify the memory field to or from which the data will be transferred via the memory extension control.

2.5.2.8 DECtape Flag - This flag, which is constantly referred to in the function descriptions, is set after specified operations are completed. It can be cleared by setting a zero into status A bit 11, and will cause an interrupt if that facility is enabled by status A bit 9.

2.6 PROGRAMMING DECTAPE

In this section, a number of simple programming examples are given to illustrate the principles outlined earlier. The PDP-8 programming library makes available many subroutines which are easily incorporated into a user program, so that the user rarely needs to develop his own DECtape handler.

In each example, it is assumed that there are no other programs in memory, and that the DECtape being used has been formatted. The examples are written in PDP-8 Assembler language.

2.6.1 Example 1: Rewind Tape

Assume that a DECtape transport number 5 has run into the forward end zone and must be rewound to the reverse end zone. A subroutine to do it looks like this:

```
Tag         Instruction         Remarks
RWND,       0
            CLA                 /Clear the accumulator
            TAD (5604           /Get the status A code
            ION                 /Turn on interrupt
            DTCA                /Clear status A register
            DTXA                /Load status A with 5604
            ION                 /Turn on the PI facility
            JMP I RWND          /Go back to main program

0           0                   /This is the interrupt
1           JMP FLAG            /service routine.

FLAG,       DTSF                /This is the skip chain
            JMP. + 2            /where the DECtape flag
            JMS DECTPE          /is discovered. The
            HLT                 /program halts if the DECtape flag is not
                                /set. When the program was started,
                                /it was assumed that no other device
                                /was on. The halt indicates an erroneous
                                /interrupt by a truant device.

DECTPE,     0
            CLA                 /Clear accumulator
            DTRB                /Read status B
            AND (1000           /Mask out all but the end of tape error
            SNA                 /Skip if a bit is in the AC
            HLT                 /See following note
            CLA                 /Clear the accumulator
            TAD (0600           /Get the new status A function
            DTXA                /Exclusive OR it onto the
                                /status A register. This
                                /will simply clear all flags,
                                /stop the DECtape and set its motion to forward.
            JMP I RWND          /Go back to the mainsubroutine.
```

NOTE

During a move function, only an end of tape error can arise. If an interrupt occurs and no such error is posted, a malfunction is indicated, and the program is halted.

2.6.2 Example 2: Find a Block

If transport number 3 is stopped near the forward end zone and must be moved to block number 5 (the current address register is CA and the word count register WC), the procedure is to put the controller into search mode normal, find out where the unit is, subtract five from that block number, set the two's complement of the result into the WC register, and place the controller into search continuous mode. The next interrupt should occur when the tape reaches block number 5. The subroutine is called SRCH.

```
Tag         Instruction         Remarks
SRCH,       0
            ION                 /Turn on the PI
            CLA
            TAD (3614           /Status A code for search, etc.
            DTCA                /Clear status A
            DTXA                /Load status A
            JMP I SRCH          /Return to subroutine

0,          0000

1,          JMP FLAG

FLAG,       DTSF                /This is the same skip
            JMP. + 2            /chain coding as in the
            JMS TAPE            /previous example.
            HLT

TAPE,       CLA
            DTRB                /Read status B
            DCA TEMP            /Store it away
            AND (0001           /Mask for DECtape flag
            SZA                 /Flag is on
            HLT                 /No flag - something is wrong
            CLA
            TAD TEMP            /Return status B
```

```
Tag             Instruction         Remarks
                AND (1000           /Test for the error flag
                SZA
                JMP ERROR           /Go to error subroutine
                JMP BLKNO           /Go to subroutine to get block number

BLKNO,          CLA
                TAD I CA            /Get block number
                TAD (7773           /Test for block 5
                SNA                 /Skip if not zero
                JMS WRT             /This is block 5 - start writing
                CLA                 /Not block 5
                TAD (5              /Get a 5
                CIA                 /Get 2's complement of 5
                TAD I CA            /Add present block number
                CIA                 /2's complement it
                DCA WC              /Put result in WC
                CLA                 /Clear accumulator
                TAD (0100           /Get next status A setting
                DTXA                /Exclusive OR into status register (continuous mode)
                ION                 /Turn on PI
                JMP I SRCH          /Go back to main program.
```

2.6.3 Summary of TC08 Timing Data (All times are ± 30%)

Operation	Time
Time to Answer Break Request	Up to 33 μs (± 30%)
Data Break Transfer Rate	4.5 μs (3 cycles) per word
Word Transfer Rate	One 12-bit word every 133 μs (± 30%)
Block Transfer Rate	One 129-word block every 25 ms (± 30%)
Start Time	375 ms (± 20%)
Stop Time	375 ms (± 20%)
Turn Around Time	375 ms (± 20%)
Time to Change from Search to a Read or Write Function	400 μs

2.7 TC08 OPERATOR CONTROLS AND INDICATORS

The single switch, WRTM/NORMAL, and an array of lights are all that the operator of the TC08 controller need concern himself with. The operation of the transports is explained in their respective manuals. The TC08 switch, located on the left-hand side of the logic panel, puts the controller in write timing and mark track mode or else in normal, or every other mode, depending on the settings, SWTM or NORMAL respectively. Table 2-4 summarizes the function of each indicator. Figure 2-7 is a photograph of the indicator panel.

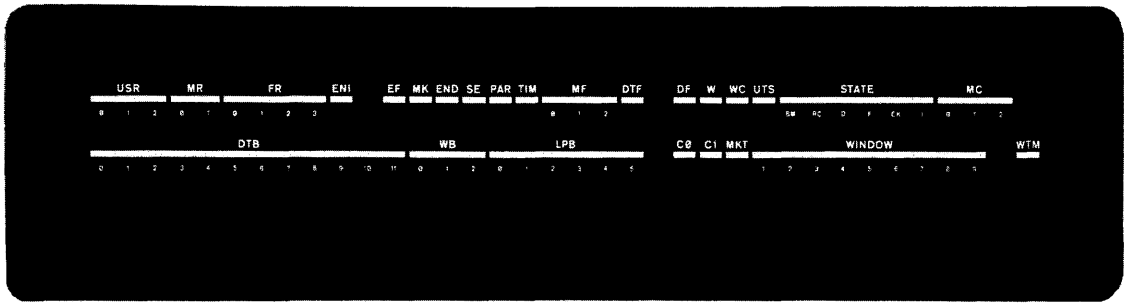


Figure 2-7 The Indicator Panel

Table 2-4
The TC08 Indicator Panel

Indicator Name	Indicator Function		
USR	The Unit Select Register specifies which transport is to be activated, according to the following table.		
	Bit State	0 1 2	Transport Selected
	0	0 0 0	8 or 0
	1	0 0 1	1
	2	0 1 0	2
	3	0 1 1	3
	4	1 0 0	4
	5	1 0 1	5
	6	1 1 0	6
	7	1 1 1	7
MR	The Motion Register specifies the three possible movements of the reel. These are:		
	Bit State		Function
	0	0 0	STOP
	1	0 1	GO REVERSE
	2	1 0	STOP
	3	1 1	GO FORWARD

Table 2-4 (Cont)
The TC08 Indicator Panel

<table>
<tr><th>Indicator Name</th><th>Indicator Function</th></tr>
<tr><td>FR</td><td>This four-bit Function Register specifies one of seven possible operations in either of two modes. BIT 0 on a 0 - normal mode.
BIT 0 on a 1 - continuous mode.
<table>
<tr><th>Bit State</th><th>1</th><th>2</th><th>3</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>MOVE</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>SEARCH</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>0</td><td>READ DATA</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>1</td><td>READ ALL</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>WRITE DATA</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>WRITE ALL</td></tr>
<tr><td>6</td><td>1</td><td>1</td><td>0</td><td>WRITE TIMING AND MARK</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>1</td><td>UNUSED (Causes select error)</td></tr>
</table></td></tr>
<tr><td>ENI</td><td>Enable the interrupt when on indicates that the TC08 can cause a program interrupt when an error flag or the DECtape flag is set.</td></tr>
<tr><td>EF</td><td>This flag is set if any one of the five following error flags come up. These conditions stop transport motion, except for the parity error of bit 4, and all cause a program interrupt if the facility is enabled.</td></tr>
<tr><td>MK</td><td>The output from the mark track instruction register is tested every time an instruction appears. If no instruction appears, this indicates that the mark track is not recorded properly and therefore an error has occurred. MK and therefore EF are set.</td></tr>
<tr><td>END</td><td>If the instruction register of the mark track decodes an end zone indicator, this flag and EF are set. A subsequent program interrupt stimulates the computer to find out what happened.</td></tr>
<tr><td>SE</td><td>This flag examines and compares various switches and status A functions, and will detect 4 incongruous combinations. These are:
a. When the transport unit select code loaded into the status A register either specifies more than one transport or none at all. This occurs when two selected transports are set to the same number, or none is set to the correct code.
b. When a write function is specified while the WRITE ENABLE/WRITE LOCK switch on the selected transport is set to the WRITE LOCK position, which inhibits writing.
c. When bits 111 are set into the function bits 6, 7, and 8 of status A, indicating a nonexistent function.
d. When the switch WRTM/NORMAL and the function register do not coincide (i.e., trying to format on NORMAL).</td></tr>
</table>

Table 2-4 (Cont)
The TC08 Indicator Panel

Indicator Name	Indicator Function
PAR	This error occurs if the longitudinal parity buffer shows an error at the end of a block during a read data function. In normal mode, the error flag is set when the DECtape flag is set. In continuous mode the error is set after the word count overflows for the block it overflows in. The parity error flag cannot be set after the DECtape flag has has been set.
TIM	This flag monitors possible timing errors, which are: a. If the data break request is not answered in 20 μs, some of the data is lost. b. If the DECtape flag is not cleared by the program before the control attempts to set it again, the condition which set it was not serviced, and was probably lost. c. If the read data or write data function is loaded into the status A register while the read heads are over a data section of the block, the complete block cannot be transferred, and an error condition is present.
MF	These three lights show the contents of the memory field register.
DTF	This light reflects the state of the DECtape flag.
DF	The Data Flag is set when the TC08 controller needs to transfer a data word through the three-cycle break.
W	This flag, when set, indicates that a write all function is occurring.
WC	The Word Count flag is set whenever the word count register overflows.
UTS	This Up-to-Speed flip-flop is set as soon as the tape transport reaches an acceptable speed.
STATE	These bits make up the TC08 state generator, a switched-tail ring counter, which steps from an idle state through five other states and back to idle as a block passes the tape heads.
BM	Block Mark is the first bit to which the state generator moves. It is set when forward block mark is in the data buffer.
RC	The Reverse Checksum state occurs when the Reverse PCC Mark cell is encountered.
D	The Data state starts with the first block that contains data (the Reverse Final Mark) and finishes when the next-to-last data block (the Prefinal Mark) passes the read heads.
F	The Final state occurs during the last cell which contains data (the Final Mark).
CK	The Checksum State occurs when the PCC Mark cell passes the heads. During this state, the checksum is deposited in the PCC Mark, if the TC08 is writing; it checks for a parity error, if the TC08 is in a read operation.
MC	These three bits represent a three-bit switched-tail counter composed of bits MC00, MC01, MC02.
DTB	The Data Buffer holds 12 bits of data on its way to or from the computer.
WB	The Write Buffer receives data from the data buffer. It feeds the transport during a write operation.

Table 2-4 (Cont)
The TC08 Indicator Panel

Indicator Name	Indicator Function
LPB	The Longitudinal Parity Buffer calculates a checksum of data that is read from or written to the magnetic tape.
C0, C1, MKT	These are the flip-flops which constitute the counters of the timing generator.
WINDOW	The Window Register is a simple shift register which receives the instruction codes from the mark track and uses the codes to set the State Generator.
WTM	This means the SWTM/NORMAL switch is in write timing and mark track mode (SWTM).

CHAPTER 3

TC08 - TC08N LOGICAL OPERATION

In Chapter 3, the logical operation of the TC08 and TC08N controllers is explained. Because the difference between the two controllers is simply a matter of level converters, that is, the two are logically identical, the term TC08 will be used for both unless otherwise indicated.

3.1 A REVIEW OF MAGNETIC TAPE RECORDING

DECtape uses a recording technique variously known as double pulse, phase modulation, or "Ferranti logic". Because the design of the TC08 reflects this recording technique, these recording methods are reviewed in this section.

3.1.1 Magnetic Recording in General

Three basic elements are required to make and reproduce a magnetic recording:

a. A device which responds to an electrical signal by creating a magnetic pattern in a magnetizable medium.

b. A magnetizable medium which will conform to and hold the magnetic pattern.

c. A device which can detect the magnetic pattern and convert it back to the original electrical signal.

These three elements take the physical form of the record head, the magnetic tape, and the reproduce head, respectively. The addition of electronic amplification and a mechanical tape handler, produces a basic magnetic recorder. Note that the record and reproduce heads are often combined into a single read/write head.

3.1.1.1 The Physics of Recording and Reproducing - A record head is similar to a transformer with a single winding in that signal current flows in the winding, producing a magnetic flux in the core material. The core of the record head is built in the form of a closed ring; but, unlike a transformer core, the ring has a short non-magnetic gap in it. When this gap is bridged by magnetic tape, the flux detours around the gap through the tape, completing the magnetic path. The magnetic tape is a ribbon of plastic on which particles of magnetic material have been uniformly deposited. As the tape moves across the record head gap, the magnetic material,

or oxide, is subjected to a flux pattern proportional to the signal current in the head winding. When the tape leaves the head gap, each tiny particle retains the state of magnetization that was last imposed on it by the protruding flux. Thus, the actual recording takes place at the trailing edge of the record head gap. A simplified diagram of the recording process is shown in Figure 3-1.

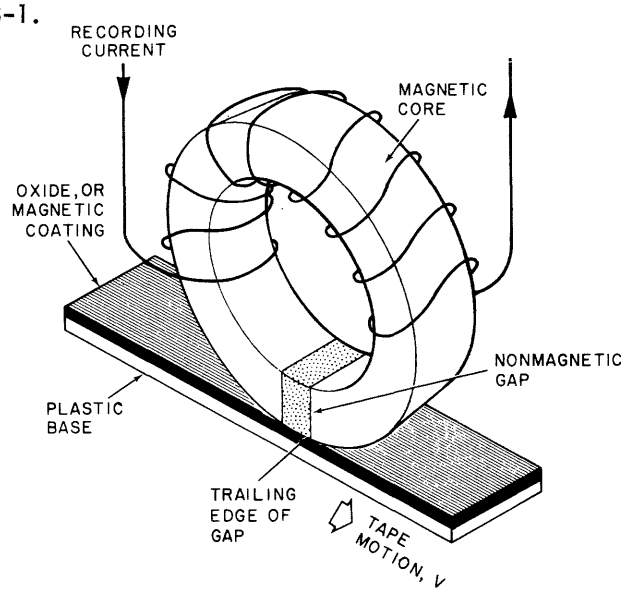


Figure 3-1 Simplified Diagram of the Magnetic Recording Process

To reproduce or recover the original signal, the magnetic pattern on the tape is moved across a reproduce head. Here again the nonmagnetic gap of the head is bridged by the magnetic oxide of the tape. Lines of flux are shunted through the core, proportional to the magnetic gradient of the pattern on the tape which is spanned by the gap. The induced voltage in the head winding follows the law of electromagnetic induction: $e = N\, d\Phi / dt$. It is important to note that the reproduced voltage is not proportional to the magnitude of the flux, but to its rate of change.

Suppose the signal to be recorded on a tape is a sine-wave voltage described by $A \sin (2\pi ft)$. The current in the record head winding and the flux Φ through the record head core will be proportional to this voltage. When the tape retains this flux pattern and regenerates it in the reproduce head core, the voltage in the reproduce head winding will be

$$e_{repro} \propto \frac{d\Phi}{dt}$$

where

$$\frac{d\Phi}{dt} = \frac{d}{dt} A \sin (2\pi ft)$$

$$= 2\pi fA \cos (2\pi ft)$$

The reproduce head acts as a differentiator so that the reproduced signal is actually the derivative of the recorded signal, and not the signal itself. This point is important, and is referred to later in the text when the principles of DECtape formatting are discussed.

3.1.2 The DECtape Read/Write Electronics

The TU55 and TU56 tape drives have 10 heads, each of which can record and reproduce. These heads are divided functionally into five pairs; one pair to record and reproduce the timing tracks, one pair for the mark tracks, and three pairs to record and reproduce the data tracks.

Figure 3-2 shows the electronics of a typical pair, consisting of two read/write heads wired in series center tapped to ground, a G888 writer, and a G888 reader. The writer is similar to a push/pull amplifier; it can drive current in either direction, depending on the relative polarity of its inputs. It can drive an almost square current pulse into the heads. The reader is a high-gain amplifier with positive feedback which will respond to a 500 μV input. It is provided with a test point which samples the output voltage of its first stage. That stage is simply a linear amplifier with a gain of 100. Subsequent stages consist of a zero crossing detector and a limiter which then drives a 7400 series TTL gate. The module is discussed in greater detail in Chapter 6.

The G888 receiver oscillates if it sees no input voltage greater than 500 μV. This characteristic is utilized by the up-to-speed logic of the timing generator (see Paragraph 3.2.1.2).

3.1.3 The DECtape Recording Technique

Suppose that a binary number 100110 is to be written on one track of the magnetic tape surface, using the electronics of Figure 3-2. Waveform A shows the current pulses in the head windings when ordinary recording is used. Since the maximum rate of current change is between 1s and 0s, during these changes the maximum flux is induced into the magnetic surface and the subsequent passage of a read head develops a maximum output voltage (B). A long string of 0s or 1s tends to look like one long 0 or one long 1.

It is possible to decipher such signals, but it is much more desirable to provide a writing technique that causes some positive action in the center of each bit time. This is accomplished by changing the phase of the writing current pulse in the middle of a bit time. The method is called phase modulation.

To produce phase modulation, the normal steady state logic to be stored must be changed before it reaches the write head. This is done by using a special write buffer (Figure 3-2). The write buffer is loaded with the bit to be written during the main timing pulse, and then complemented at a half clock pulse. (In the TC08 these are called TP00 and TP01, respectively.) The half clock occurs at the same frequency as the main clock, but it is displaced by 180 degrees. The effect is to place a wave of flux on the tape as it passes beneath the head. The polarity of this wave depends on the bit which is loaded during the main clock pulse, which, in turn, depends on whether it was a 0 or a 1.

The read voltage is amplified and clipped in the reader. It is then gated with the half-clock pulse into the data flip-flop, yielding the written version delayed by half a clock time.

Notice that the voltage readout peaks near the center of each bit time, whether a string of 0s or 1s occurs or not. The choice of polarities is arbitrary, but there is a distinct 180-degree difference between a 0 and a 1 readout.

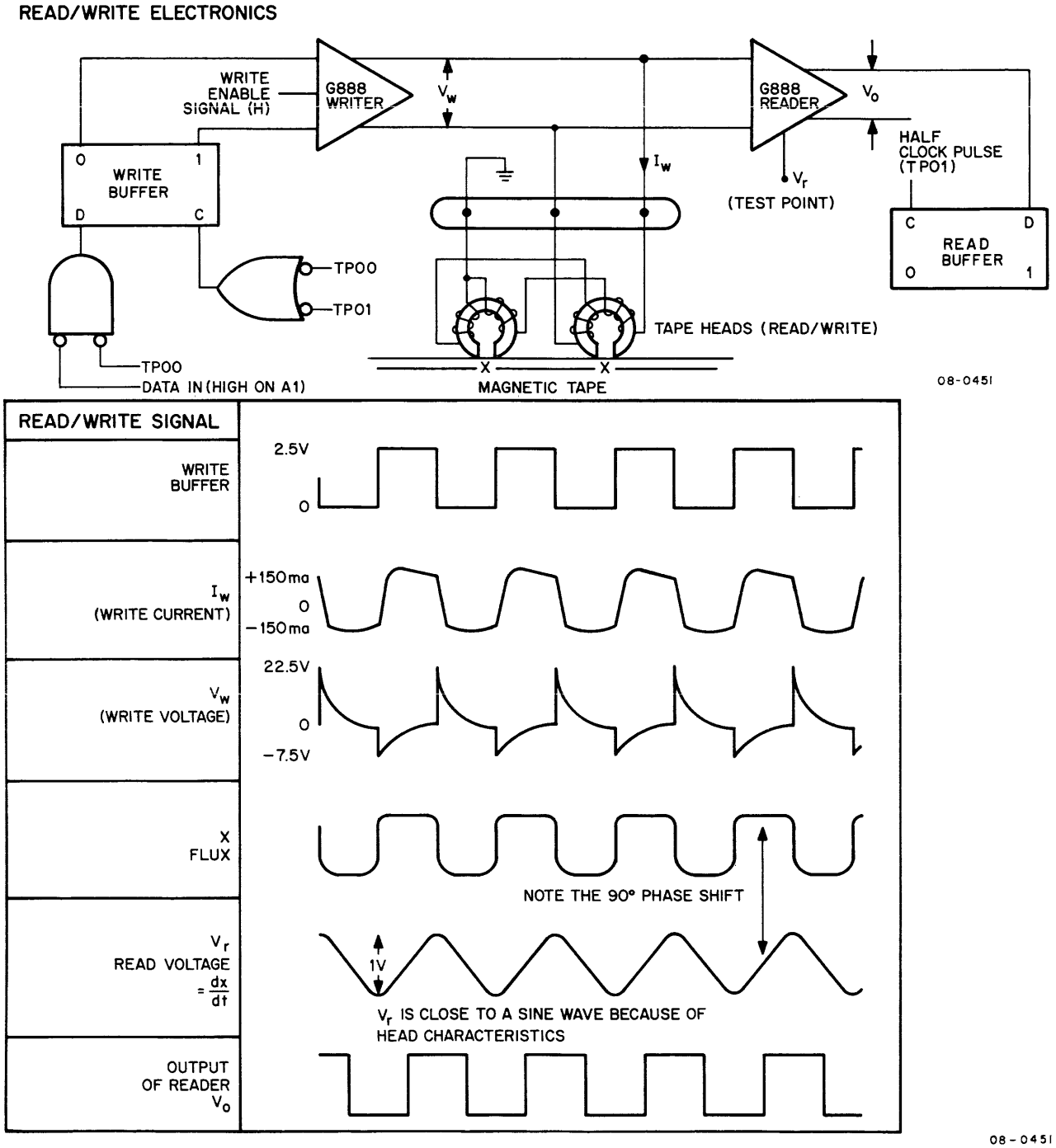


Figure 3-2 DECtape Read/Write Electronics and Waveforms

3.2 THE DECTAPE SYSTEM

In this section, the TC08 controller is divided into subunits, and each subunit is analyzed. The subunits are so interrelated, however, that it is impossible to present them in any order of appearance which will not require the text to reference sections not yet mentioned. The reader is urged, therefore, to read the chapter several times, and keep in mind the overall block diagram.

The DECtape system comprises a controller, the TC08, and up to 8 TU55 or 4 TU56 transports. Each transport contains a tape deck with reels, reel motors, tape guides, and 10 read/write heads. It also includes a rotary selection switch and several functional switches. For complete descriptions of the transports, refer to their respective manuals.

The logic circuits of the transport command tape movement in either direction over the heads. These circuits can be controlled by the TC08 under the direction of its status register.

3.2.1 The DECtape Controller

A block diagram of the DECtape TC08 controller is shown in Figure 3-3. It consists of a 12-bit command register, a 6-bit status register, a 12-bit data register, a 6-bit parity register, a 6-bit state generator, a 9-bit window register, a timing generator, and the I/O logic. The command register selects the mode of operation (read or write), the transport which is to operate (transport 6), and the direction of tape motion. The data register buffers the information between the computer and the transport, while the parity register holds the checksum. The window register decodes the mark track and sets the state generator into the correct modes (data, parity, block number) according to the position of the tape over the heads.

The timing generator writes the timing track during write timing and mark and reads it back during ordinary operation. It contains a set of counters which overflow after every 4 lines, or a 12-bit word, and after every 6 lines, or a complete mark track cell. These counters, together with the timing pulse, regulate all the other blocks.

The status register records any timing or parity errors which occur during operation. The I/O logic posts a data flag (DF) when the controller wants to transfer data through the 3-cycle break to or from memory, and the DECtape flag (DTF) whenever an operation has been completed.

3.2.1.1 The Command Register - A simplified diagram of the command register and the tape drive it controls is shown in Figure 3-4. It is divided into 4 sections: the unit select register, whose code must match the unit select switch code of the transport; the motion register, which sets the motion and direction flip-flops of the

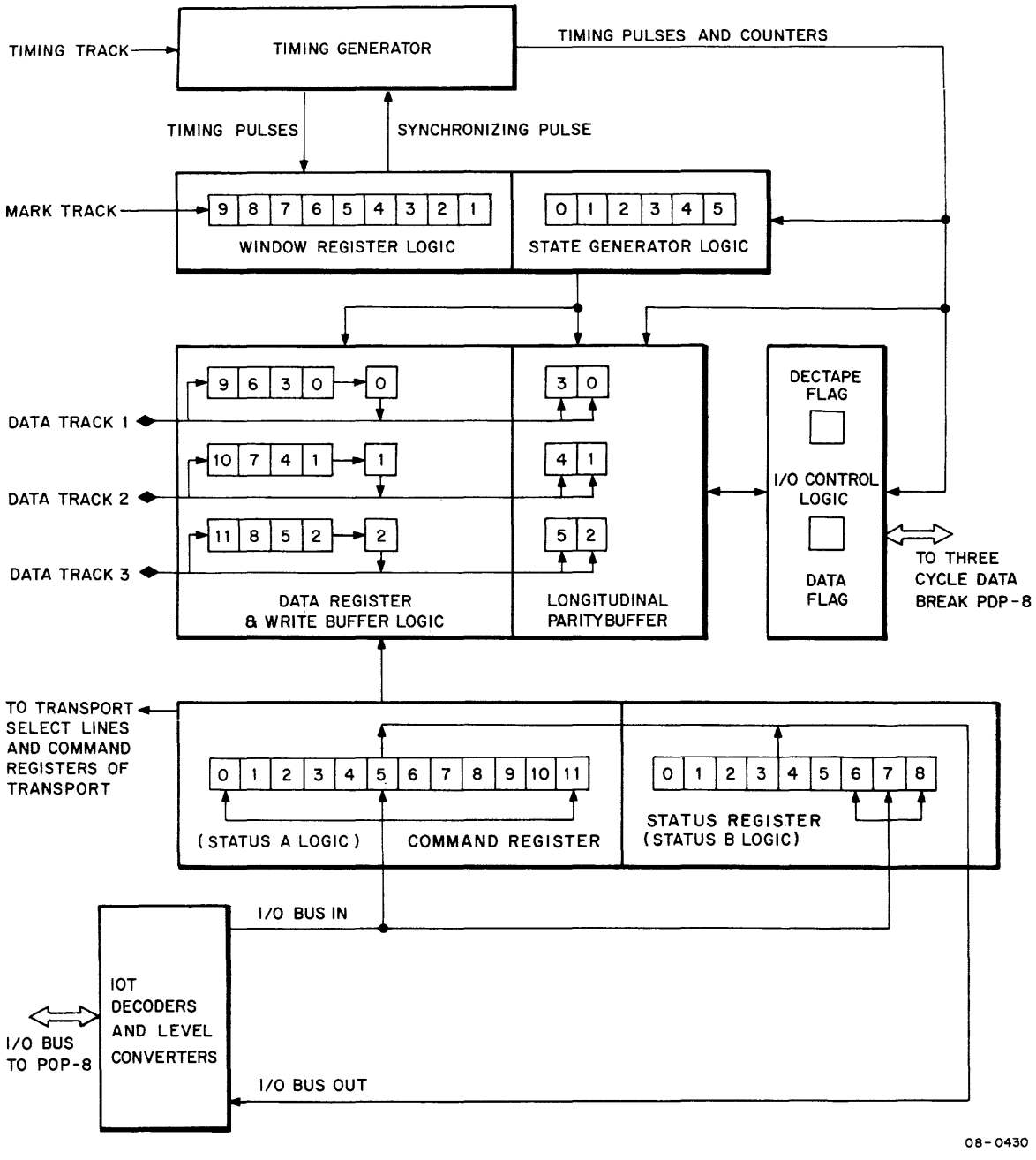


Figure 3-3 The TC08 DECtape Controller Block Diagram

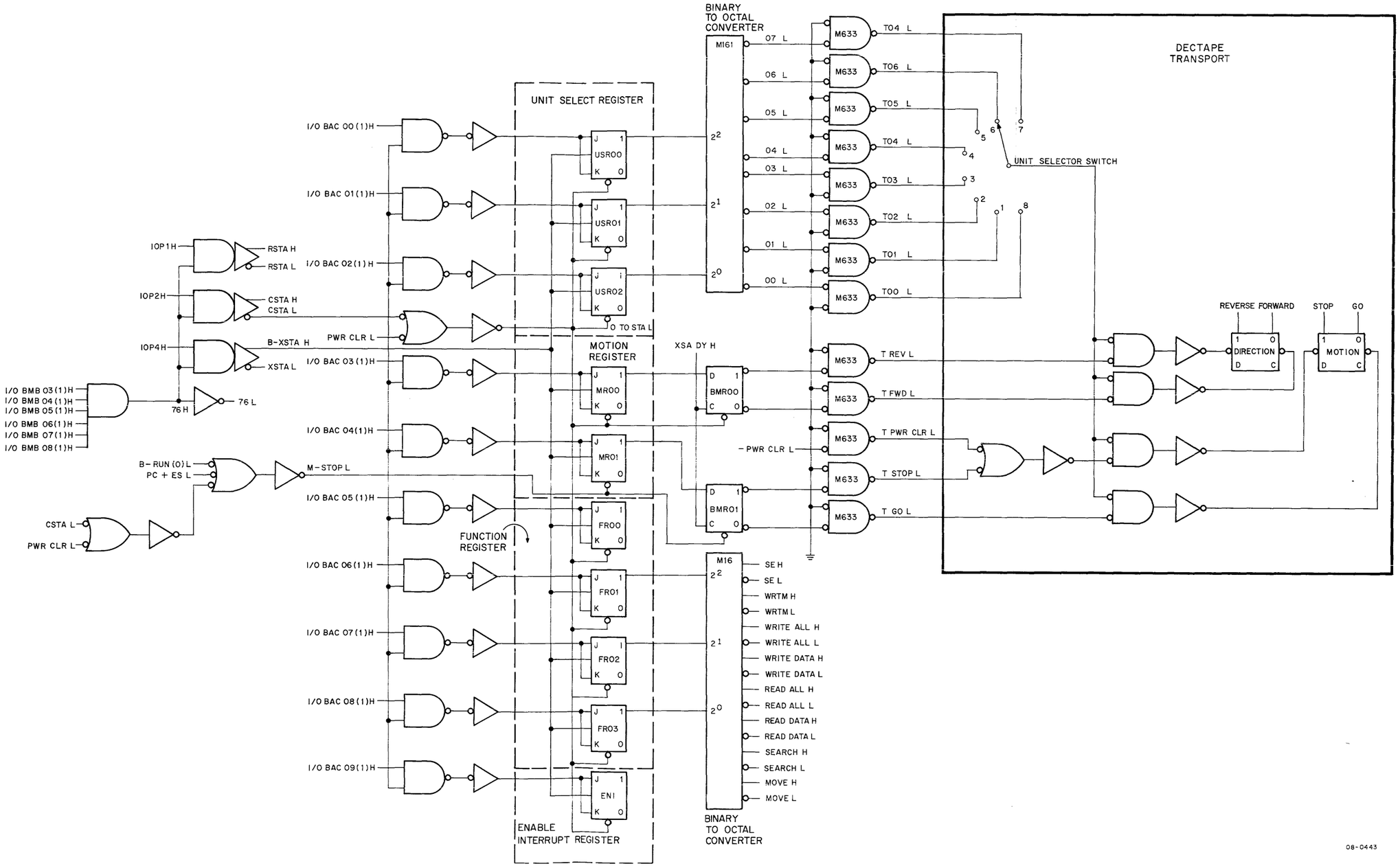


Figure 3-4 Command Register

selected transport; the function register, which is decoded to determine in which of the seven modes the controller will operate; and, finally, the enable flip-flop, which, when set, allows the controller to post a program interrupt request to the computer. The motion register is double buffered so that its effects will not be felt until the unit select register has established itself on each transport. Without this delay, two transports could pick up the same motion command.

Each of the flip-flops in this register is a JK which will complement whenever its appropriate input line is asserted and the XSTA pulse issued through the IOT instruction. The buffered motion registers are D-type flip-flops which are jammed with the delayed XSAD pulse, XSA DY H.

Device code 76 with IOP 2 complements selected flip-flops, and code 76 with IOP 4 (CSTA) clears all. Figure 3-5 shows the timing for the various versions of the PDP-8.

Flip-flops MR01 and BMR01, which select the stop or go function, clear and stop the transport if a CSTA is issued, if power clear is issued, if the computer stops (B - RUN(0) L appears), or if any error except a parity error occurs (PC + ESL).

3.2.1.2 The Timing Generator - This part of the controller (shown simplified in Figure 3-6) has 4 subsections; the timing track write logic, the up-to-speed logic, the timing track read logic, and the counters.

The timing track write logic is used only when a tape is being formatted. Its M401 clock is enabled when the switch is on SWTM and this mode is selected. This 120-kc clock starts a two-bit switched tail counter CK00, CK01. CK00 is used to write the timing track, and CK01, 90 degrees out of phase, generates the internal signals to the controller for writing the mark track. The reason for this arrangement is worth further explanation. The timing signals that are being recorded now will later be read back and used to read and write data. We know from previous theory that these timing tracks will read back 90 degrees out of phase from when they were written. So that the mark track being written corresponds in phase to the data to be written later, the mark track must be written 90 degrees out of phase with the presently generated timing track. This is accomplished by using CK00 to write the timing track, but CK01, which is 90 degrees out of phase, to write the mark track.

The up-to-speed logic prevents timing pulses from entering the main controller until the tape motion has reached an acceptable speed. It does this by monitoring the frequency of the timing pulses coming off the tape with two delays. As noted in Paragraph 3.1.2, the G888 reader oscillates if it detects no input signal above 500 μV. The first delay, which is fired whenever the computer requests a change of transport or motion, allows the tape to reach a speed at which the G888 stops oscillating and starts responding to the timing track (120 ms). The next delay, an integrating-one-shot, fires only after the timing track signals reach a specified frequency and the first delay has timed out. This sets the up-to-speed (UTS) flip-flop. Gates (3) are enabled, and timing pulses TP00 and TP01 are passed on to the rest of the generator.

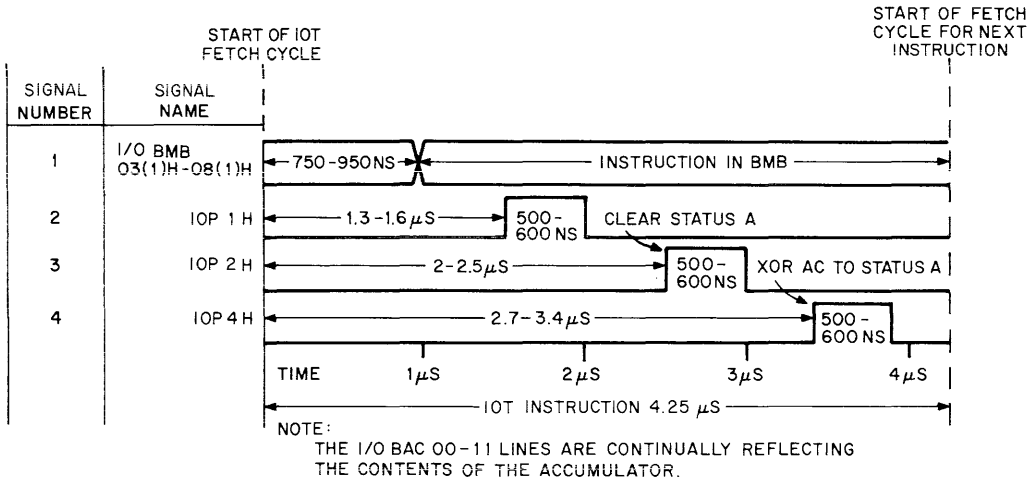


Figure 3-5A Command Register Timing with PDP-8/L

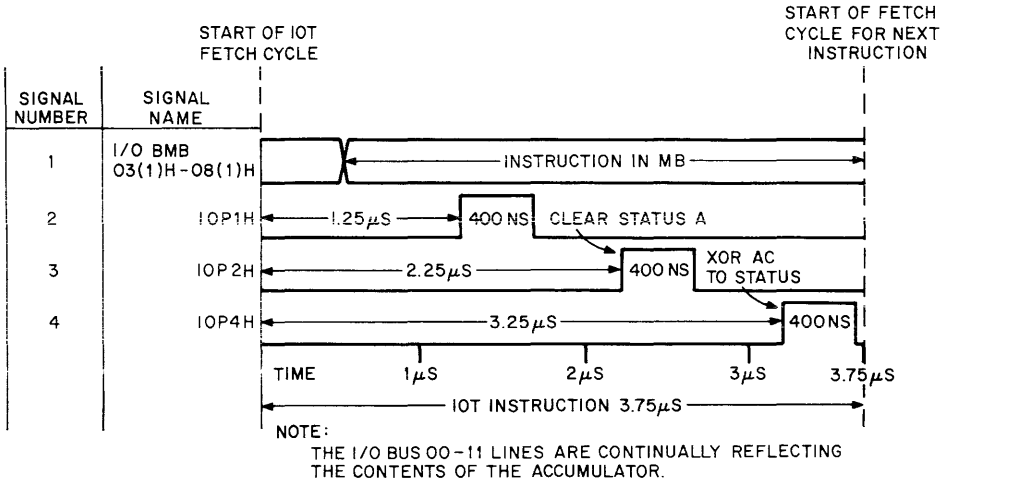


Figure 3-5B Command Register Timing with PDP-8

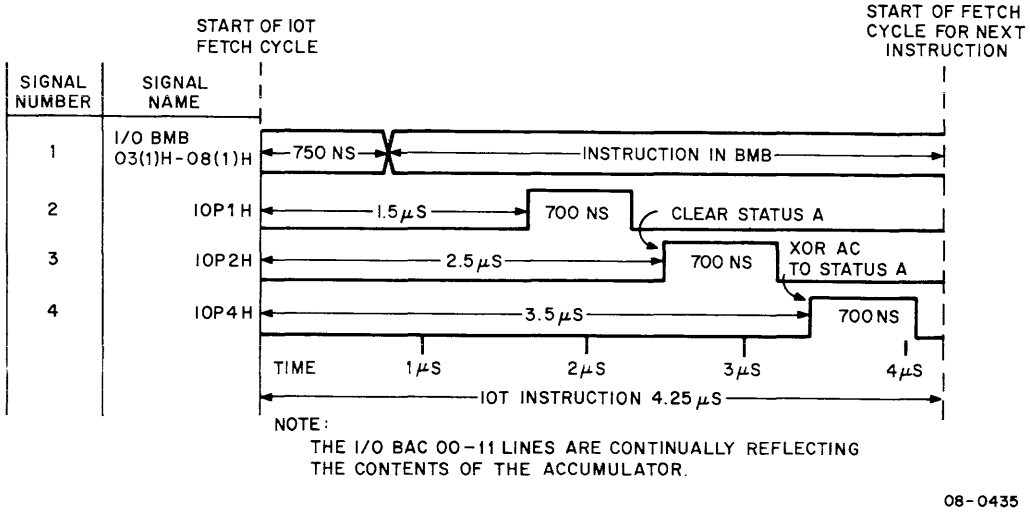


Figure 3-5C Command Register Timing with PDP-8/I

The timing track signal is received by the G888 reader, which then generates two complementary signals T TRK (0)H and T TRK (1)H on the leading and lagging edges of the timing pulse. If the controller is not in Write Timing and Mark Track Mode, gates (1) are enabled, and these signals each trigger their respective 10 μs delay. These delays serve two functions: they do not accept any other pulses for their period, thus eliminating any noise which may follow the pulse; and they also disable their opposing signal at gate (3), thus eliminating any possible crosstalk between the two. Finally, if the controller is in Write Timing and Mark Track Mode, gates (2) are enabled, and the counter CK01 generates the proper timing pulses.

Finally, the timing pulses feed two sets of counters (see Figure 3-7), C00 and MKT, which trigger on TP00 and are used to keep track of the number of bits that have been read from or written into a track, up to 4 (which means a 12-bit word). C01 triggers on TP01 and divides its pulses by 2. The value of this will become obvious later.

The three-bit ring counter, MC00 - MC02, recycles every 6 bits per track (thus every cell). It is used to synchronize the mark track cells as they are decoded from the window register.

These counters are synchronized at gate (B) as the window register decodes the interblock sync mark (725 or 525) during search, read data, read all, or write all functions. For read all and write all this synchronizing occurs on the first block after the up-to-speed flip-flop is set, but not again until it resets.

During search and read data, the controller resynchronizes after every block.

3.2.1.3 The Window Register - This is a 9-bit shift register (see Figure 3-8) which remains cleared until the UTS flip-flop has set. It then begins to shift the mark track code in through its least significant bit. No decoding is carried out until W01, the most significant bit, is set. This bit latches on a one and decoding begins. Requiring W01 to latch before decoding guarantees that at least 9 bits have been transferred, and, therefore, that the code is a valid one. The decoding shown in Figure 3-8 is carried out for the benefit of the state generator. Decoding for other subunits is shown in their respective diagrams.

3.2.1.4 The State Generator - As the window register decodes information from the mark track, the state generator responds by interpreting the code appropriately and stepping through six states as different regions of a block appear. This process guarantees that a block of data is handled completely; that is, that the controller does not start writing half way into a block because it has detected a data region on the mark track.

The state generator in Figure 3-8 is 6 bits long. It starts off in the idle state and steps from that through a start block, a parity check, a data, a final, and a checksum state, as a complete block passes the read heads. It cannot leave the idle state unless it sees the beginning of a block, so there is no chance that a block will be partially written into or read.

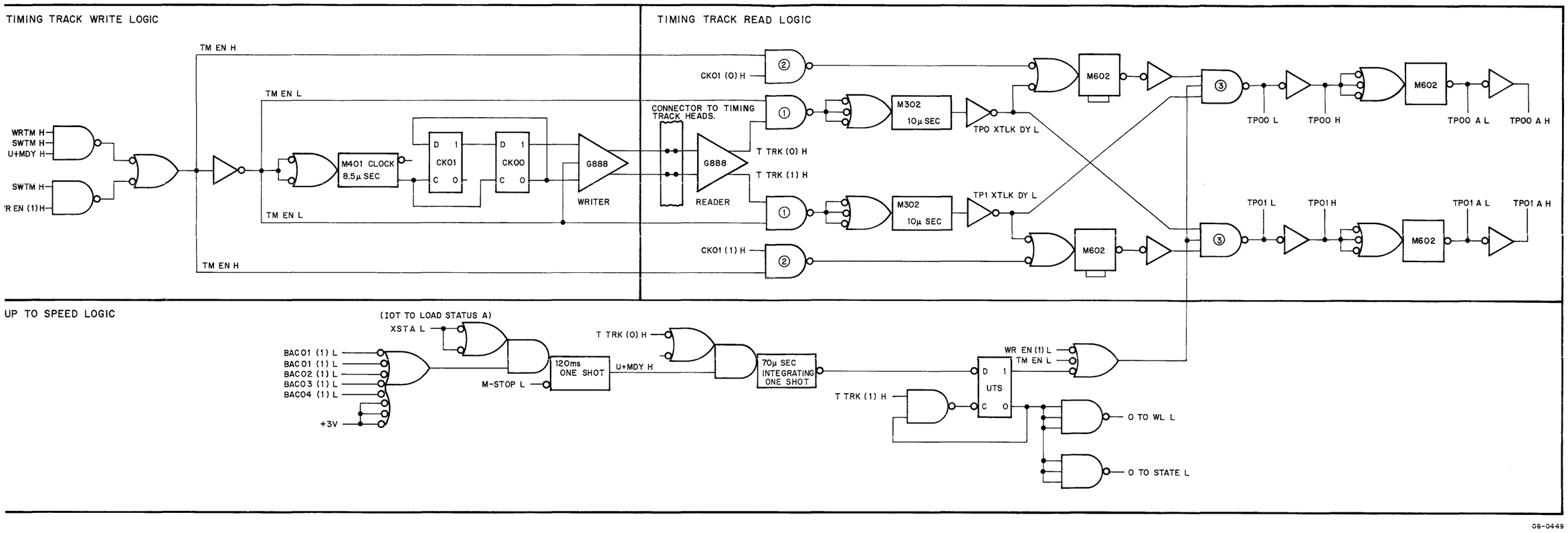


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Figure 3-6 Timing Generator

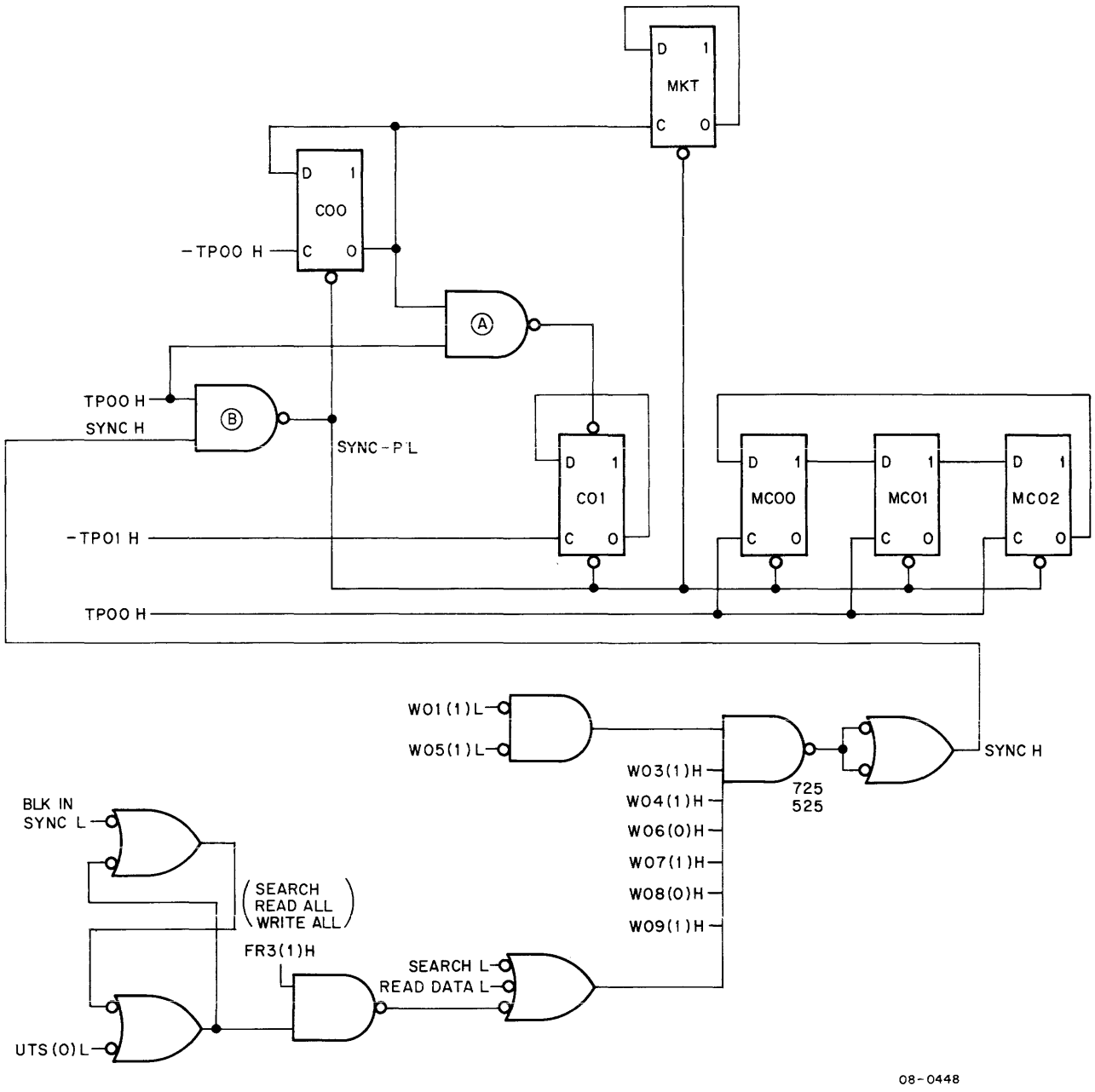


Figure 3-7 The Counters

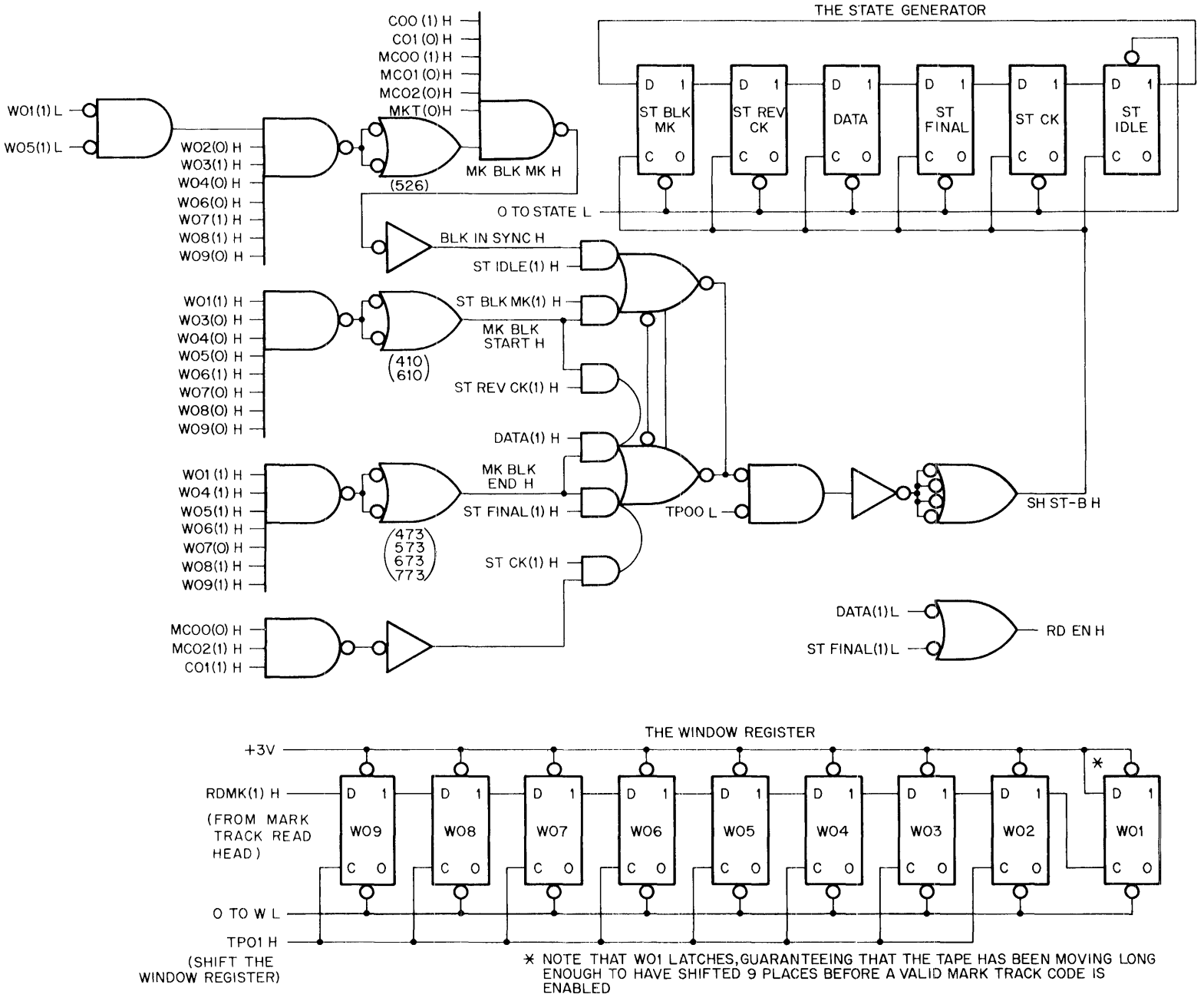


Figure 3-8 The Window Register and State Generator

Table 3-1 shows the relationship between the window decoding and the mark track, and their functions within the controller. Note that the mark track code over any given cell depends on the direction of motion of the tape. If the tape is reversed, then the mark track codes are transformed into their obverse complements; i.e., 73 → 10, 51 → 32, 45 → 26, 70 → 70, and 25 → 25. The result is the same order of codes on the mark track regardless of the direction of the tape.

3.2.1.5 The Data Buffer - Figure 3-9 shows a simplified schematic of 4 bits of the 12-bit data buffer. During a read operation, the data buffer shifts the output of the three read heads into three 4-bit shift registers at time TP01. When the buffer fills, the data flag is set (I/O LOGIC) and the buffer is transferred into Memory.

During a write operation (when Write Enable (WR EN (1)) is asserted), the data buffer is loaded from memory, then alternatively shifted into the three-bit write buffer which is complemented on TP01. The direction of the transition during complementation determines whether a 1 or a 0 has been shifted into the word buffer, and thus what is written on the data track.

At the end of a block during a write operation, the LPB (parity register) is jammed into the data buffer and word buffer and written into the appropriate cell. During a read operation, the parity register is tested for possible error.

Timing diagrams for these operations are discussed later.

3.2.1.6 The Longitudinal Parity Buffer - This buffer (shown in Figure 3-10) is initiated (zeroed) when the ST REV CK(1)H mark passes over the read heads. From here on each data bit complements a parity flip-flop if it is a zero. There are two sets of three flip-flops in the LPB. A set samples the incoming data tracks every alternate timing pulse. When the end of the block is reached the result of this calculating is either deposited, if the machine is writing, or tested for error, if it is reading.

The error testing is done by regarding the checksum deposited at the end of the block as a data word. After this word is seen by the LPB, the LPB should be all ones, as shown in the following:

Let ↑ define the operation between data bits on any track as performed by the LPB
Let A and B represent two bits (or two strings of bits).
i.e., $A \uparrow B = \overline{A}\overline{B} + AB = C$ = checksum
Then $A \uparrow B \uparrow C = C \uparrow C = \overline{C}\overline{C} + CC = 1$

Complete timing diagrams for these operations are discussed later.

3.2.1.7 The I/O Control - All of the data transfers between the computer and the DECtape take place through the 3-cycle data break facility. The control logic which handles these transfers consists of a data flag (DF) to request the transfer, a word count overflow flag (WC) which is set when the word count overflows, and the data buffer which receives and transmits data and miscellaneous gates. Figures 3-11 and 3-12 show a simplified schematic of the logic and the associated timing.

Table 3-1
Mark Track and Window Codes

Mark Track Code	Name	Window Code	Name	Function
55	REV END MARK	555	None	This code requires no operation. It indicates that the tape is leaving an end zone.
25	INTERBLOCK SYNC	725 525	SYNCH H	This code is used by the timing generator to synchronize its counters with the beginning of a block. It occurs between blocks and at either end of the tape.
26	FORWARD BLOCK MARK	526	MK BLK MK	This code occurs when the block number is in the data register. During a search, the DF is set and a transfer is carried out. This code also steps the state generator from IDLE to ST BLK MK.
32	REVERSE GUARD MARK	632	MK DATA SYNC	This is a no-operation code which gives the computer time to respond to the block number it has found in 26.
10	LOCK MARK	610	MK BLK START	This code steps the state generator from ST BLK MK to ST REV CK (Reverse Checksum). During this state, the LPB is initiated.
10	REVERSE PCC MARK	410	MK BLK START	The same code also steps the state generator to DATA; the controller then carries out data transfers.
10	REVERSE FINAL MARK	410	MK BLK START	No action is taken on this code here, except that the controller checks to be sure it is decoded. The first data block is happening.
10	REVERSE PREFINAL	410	MK BLK START	Again no action is taken. This indicates the second data block is happening.
70	DATA MARK	470	MK DATA	These codes indicate that a data cell is under the heads.
73	PREFINAL MARK	473	MK BLK END	This code indicates that the last data cell is about to happen. The state generator switches to ST FINAL.
73	FINAL MARK	773	MK BLK END	This indicates that the last data cell has passed the heads. The state generator switches to ST CK (Checksum) to deal with the parity checksum. Then the state generator goes to IDLE.
73	PCC MARK	773	MK BLK END	The longitudinal parity checksum is stored in the PCC MARK cell. No operation occurs when MK BLK END is decoded.
73	REVERSE LOCK MARK	773	MK BLK END	No operation.
51	GUARD MARK	751	------	No operation. This code becomes 32 when the tape is travelling in the opposite direction. In this direction it does nothing.
45	REVERSE BLOCK MARK	545	------	No operation.

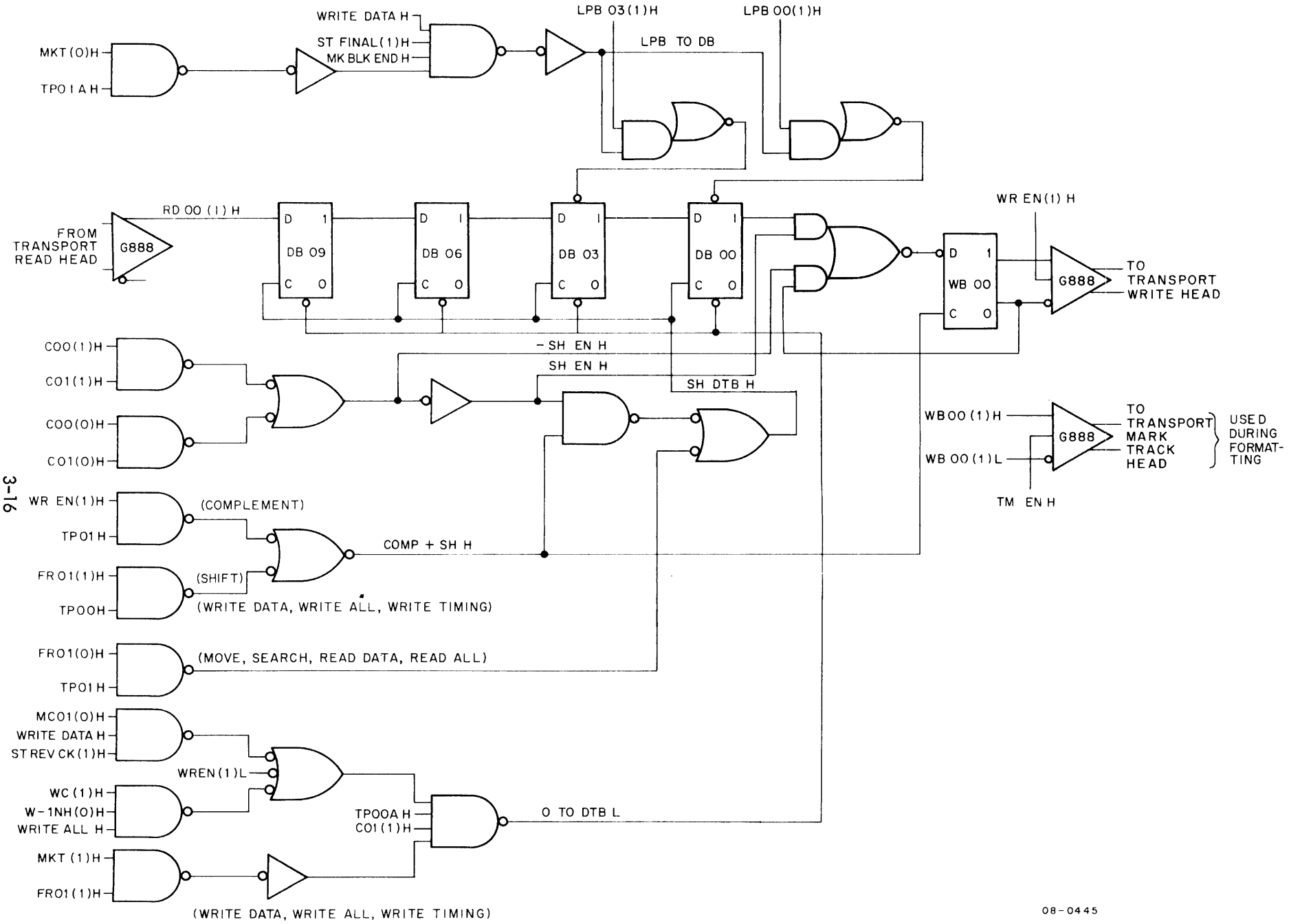


Figure 3-9 Data Buffer

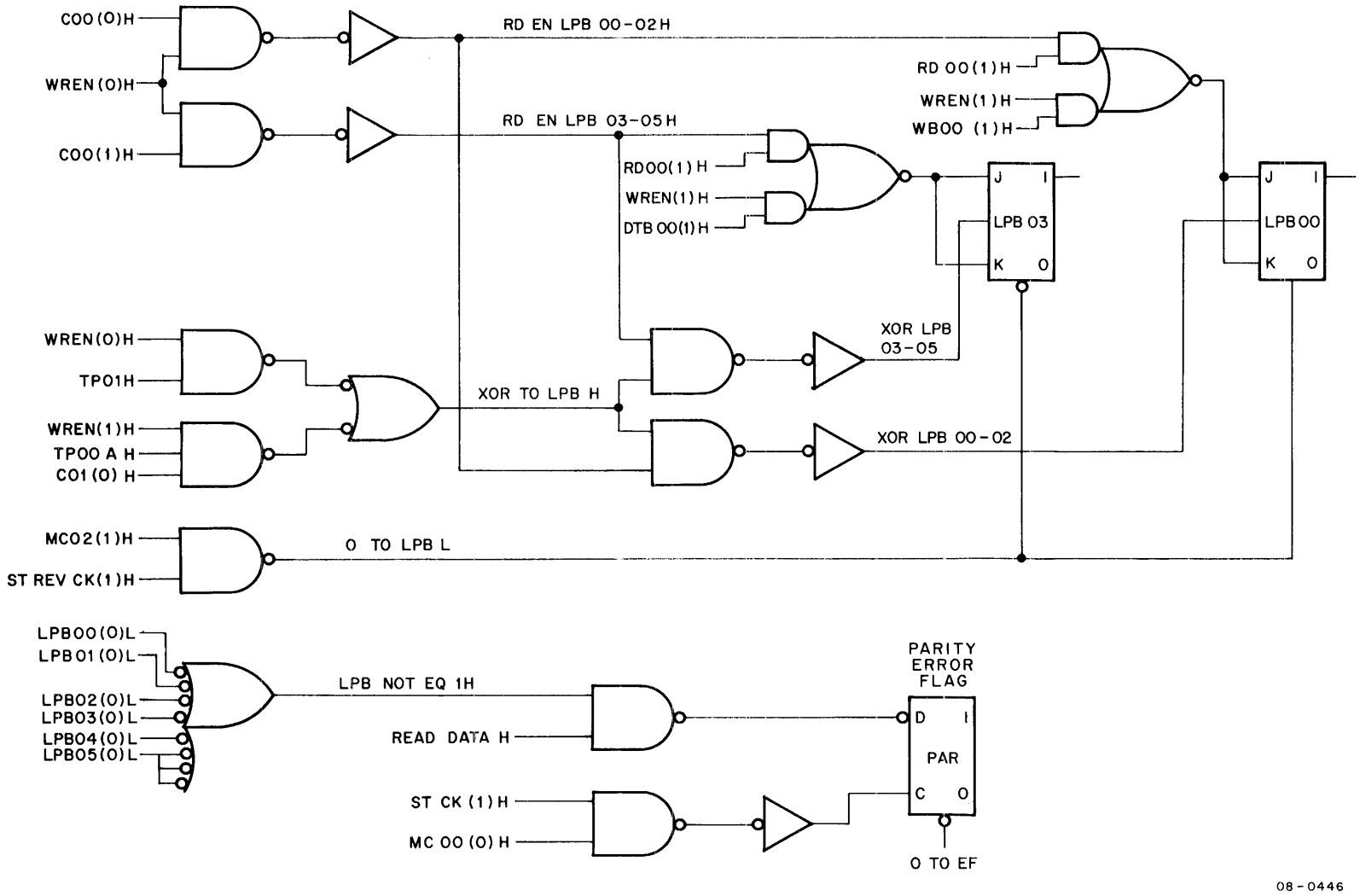


Figure 3-10 The Longitudinal Parity Buffer

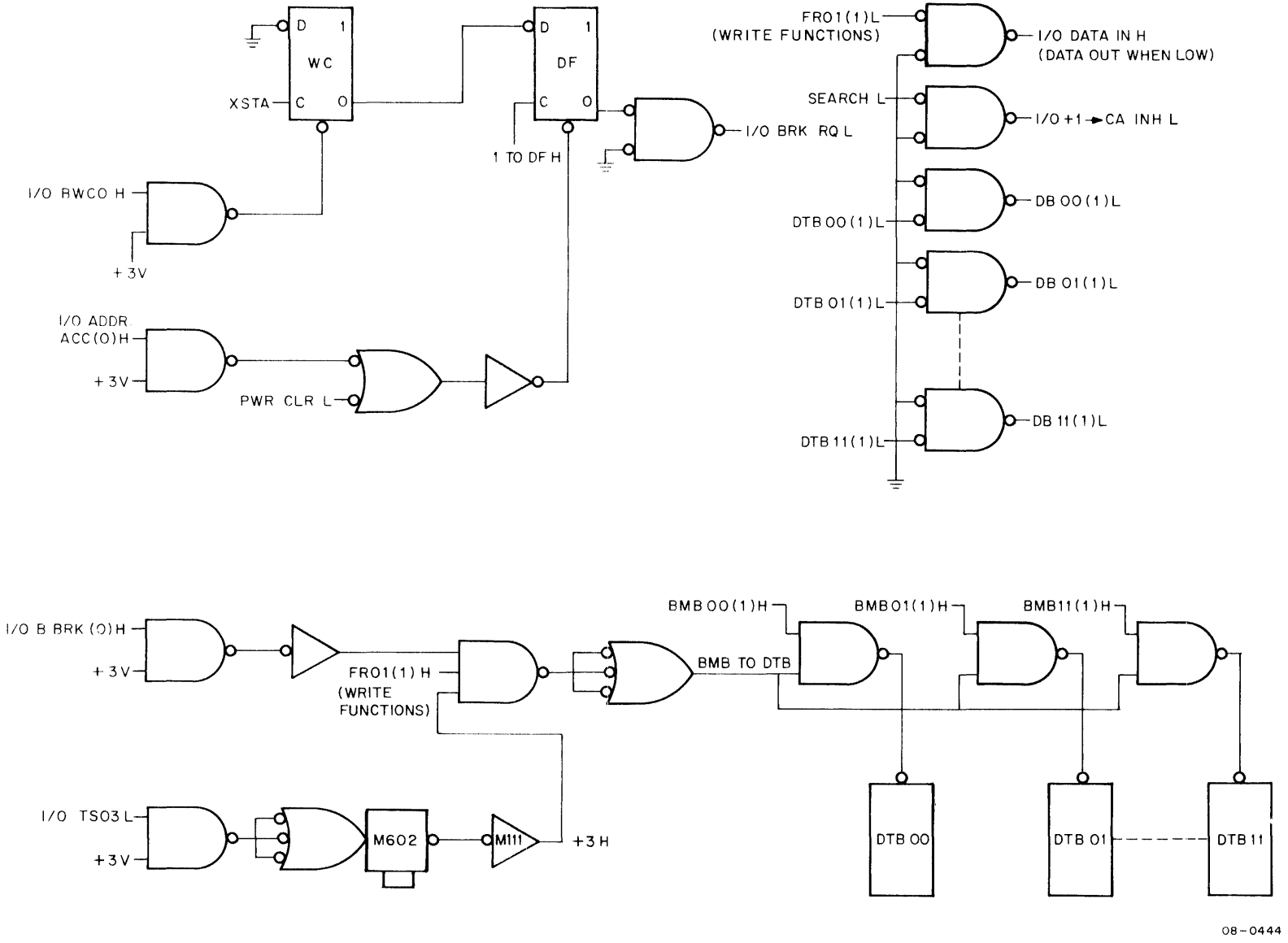


Figure 3-11 The I/O Control

When the computer uses more than 8K of core, it adds a memory extension control. In order to address more than 8K, the I/O Control uses a memory field register which is set by the program and supplies the current address extension to Memory Extension Control input EA00 L →EA12 L.

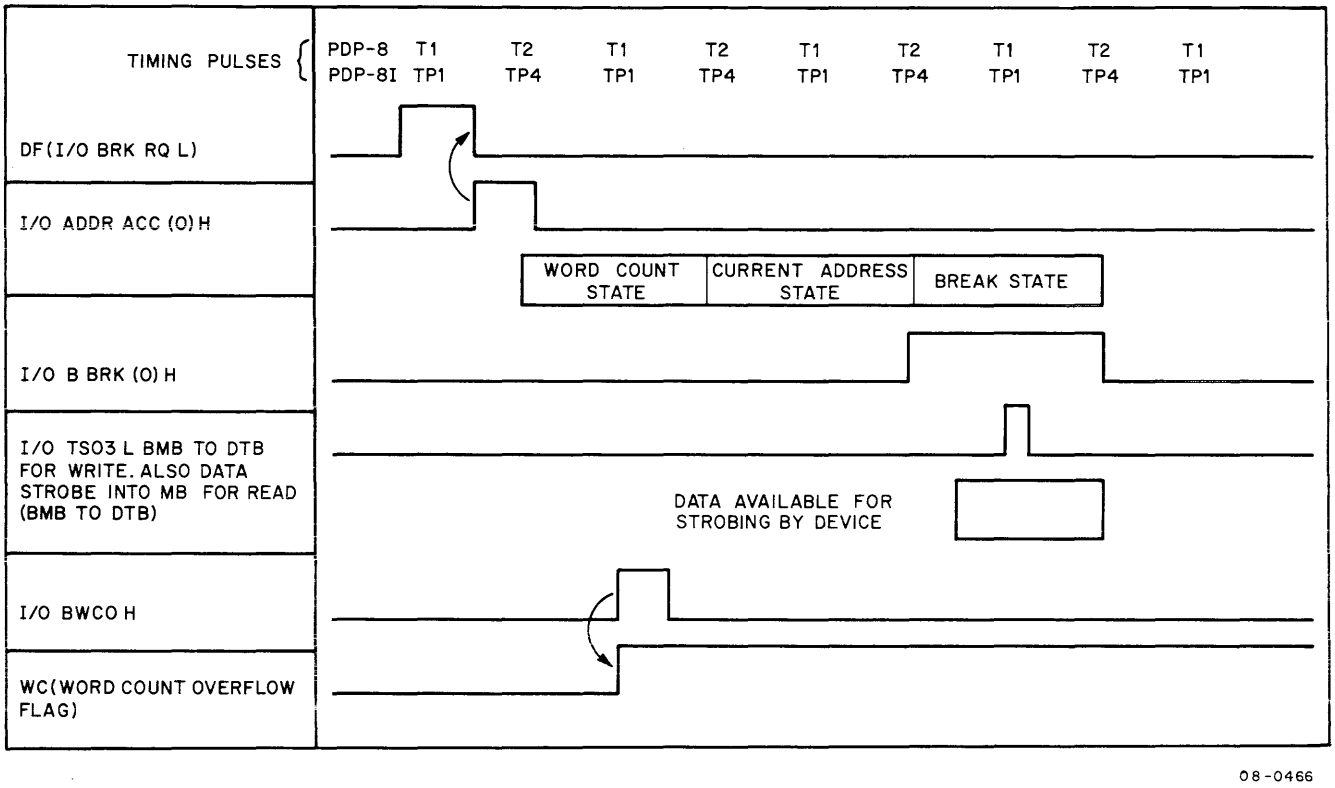


Figure 3-12 The I/O Control Timing

The DECtape (DTF) flag (Figure 3-13) is set at the end of each operation; this causes a program interrupt to the computer if the enable interrupt flag (ENI) is also set. The DTF is reset with the XSTA IOT instruction. Engineering drawing D-BS-TC08-0-4 shows the logic which sets the DTF.

3.2.1.8 The Write Enable Flag - One piece of logic which does not fit into any of the foregoing subsystems, but plays an important role in the operation of the control, is the WREN (Write Enable) flag (see Figure 3-14), which is set whenever the controller is writing information on the tape. This flag enables the write amplifier; the conditions under which it is set are summarized in Figure 3-14.

3.2.1.9 The Status B Logic (see Figure 3-15) - The status B logic consists of the error flags (Sheet 1) and the memory field logic (Sheet 2). Table 3-2 summarizes the logical reasons for each of the errors. The functional significance is discussed in Chapter 2.

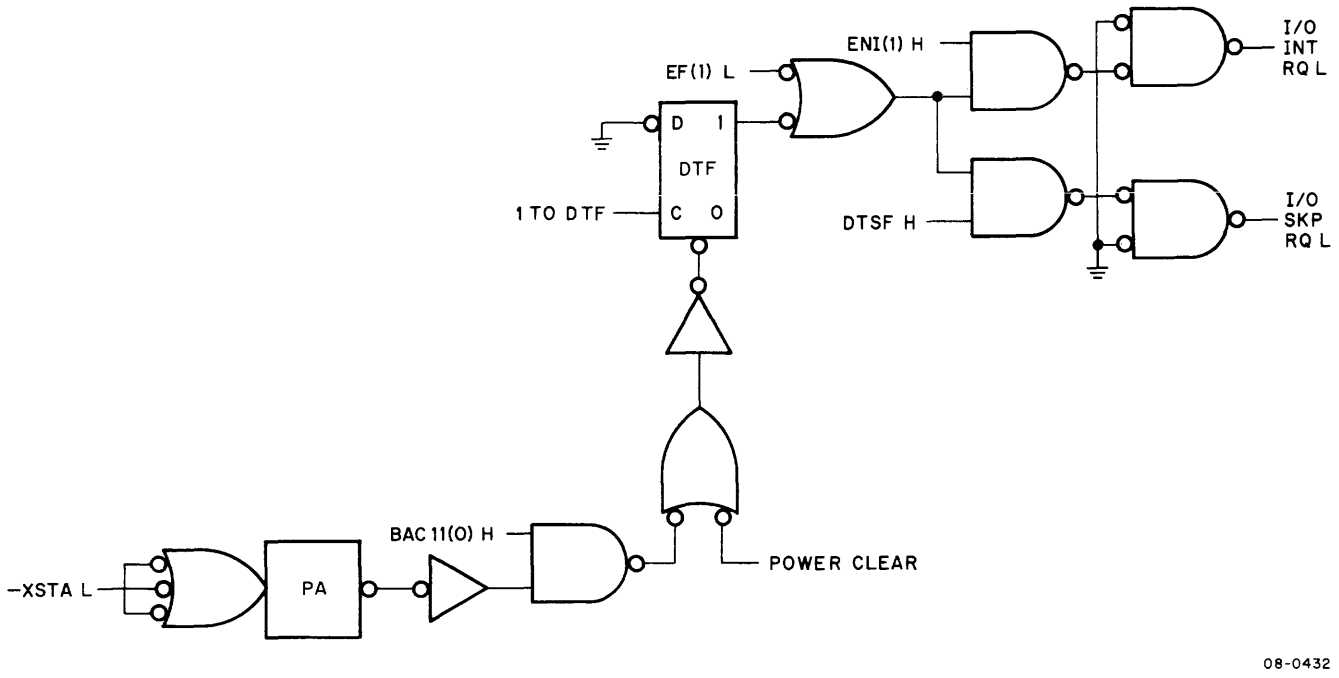


Figure 3-13 The DECtape Flag

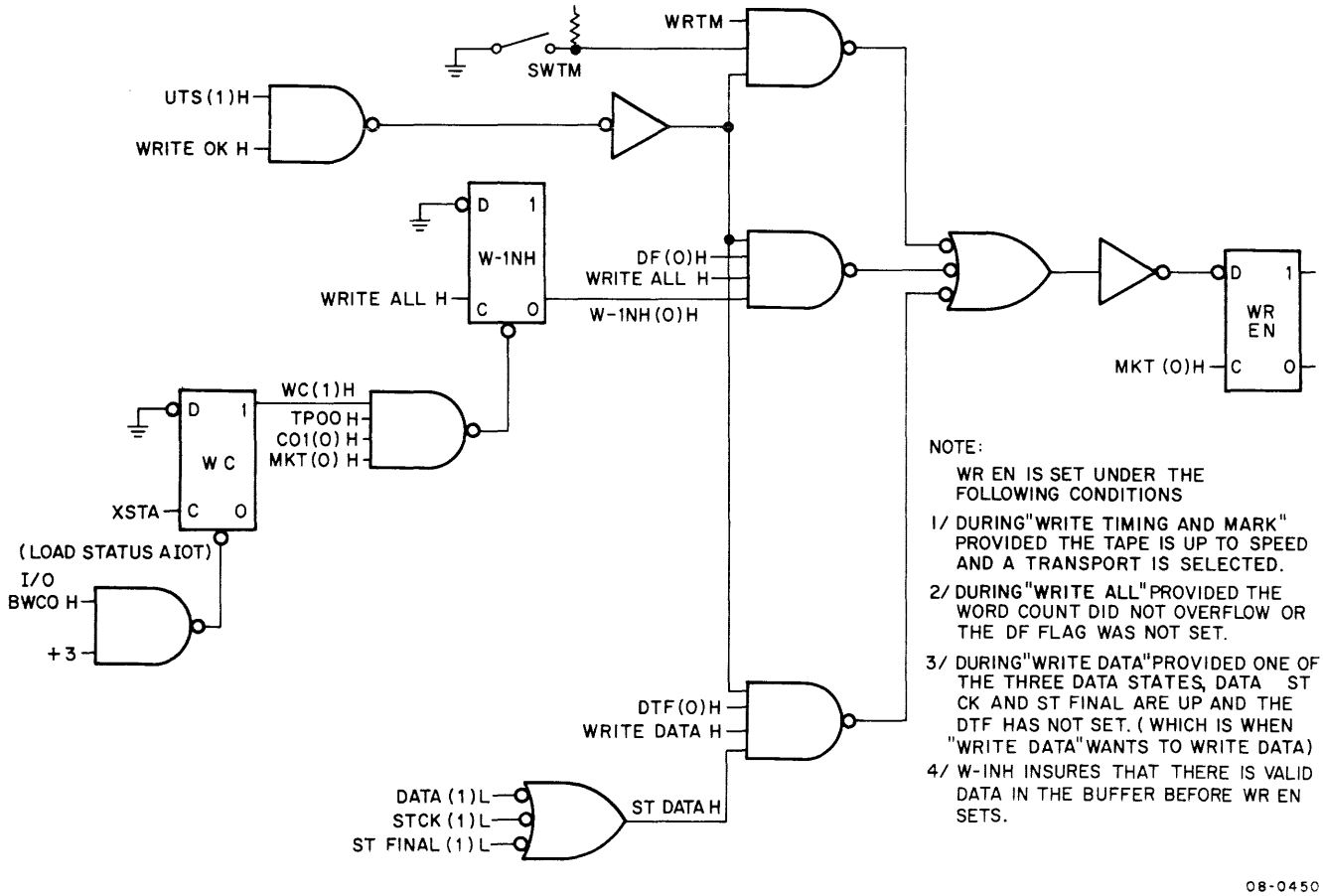


Figure 3-14 The Write Enable Flag

Table 3-2
The Error Flags

Flag	Function	Conditions When It Is Set
MKTK	MARK TRACK ERROR	This error occurs if the window register decodes a MK BLK START, a MK DATA, a MK BLK END, or a MK END during any other but BLK MK or IDLE states, unless the transport is in a move mode.
END	END OF TAPE	When the MK END code shows up in the window register, it signifies that the tape has gone into the forward end zone. This flag is posted.
SEL	SELECT ERROR	A select error occurs under any of three conditions: (1) If the write timing and mark track function and the SWTM switch are not selected or unselected simultaneously. (2) If a write function (FRO1(1)) is selected by the write enable switch and is not selected on the transport (-WRITE OK). (3) If no transport is selected; i.e., if no select switch of a transport corresponds to the number in the unit select register, or if more than one is selected. Both of these conditions are sensed by the G879.
PAR	PARITY	If, during a read operation (READ DATA), the LPB is not equal to one when ST CK occurs, then PAR is set.
TIM	TIMING ERROR	A timing error occurs under any of the following conditions: (1) If a +1 to DTF occurs while the DTF is still up, indicating that the flag was not serviced in time. (2) If the data flag is on a one when a shift data buffer pulse (SH DTB) occurs, indicating that the three-cycle break did not operate on time. (3) If an XSTA IOT occurs in any state other than BLK MK or IDLE, and the RD + WD signal is high, then the IOT occurred during a read or write operation, which should not happen.

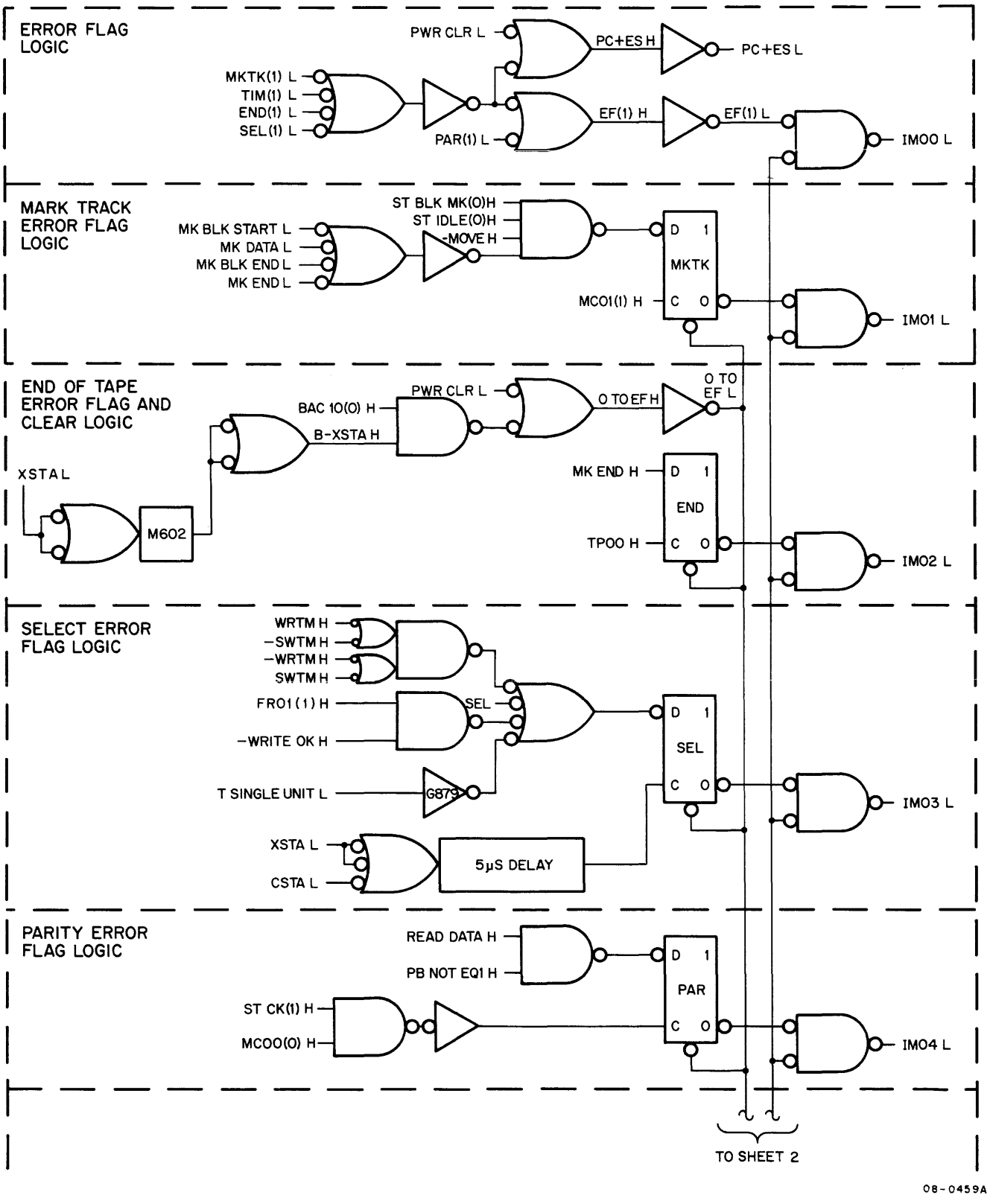


Figure 3-15 Status B Logic of the Error Flags (Sheet 1)

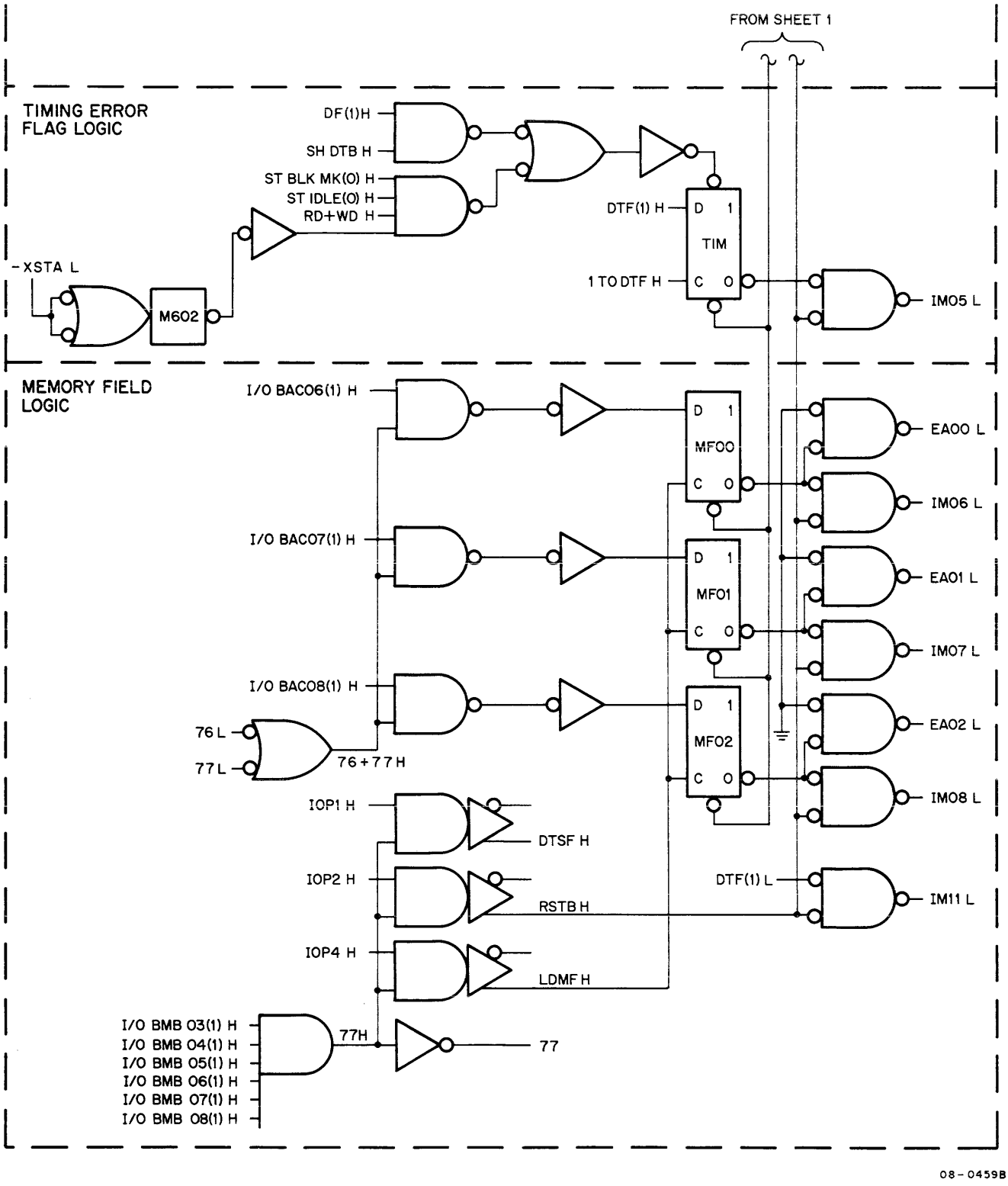


Figure 3-15 Status B Logic of the Error Flags (Sheet 2)

3.3 THE TC08 SYSTEM TIMING

In the previous section, each of the individual subsystems of the TC08 controller was studied. In this section, these units are examined as they relate to the system. Extensive timing diagrams in Figures 3-16, 3-17, and 3-18 show how the system behaves when in Write Timing and Mark Track mode, in Search mode going into Write or Write All, and in Read or Read All, respectively.

3.3.1 Write Timing and Mark Track

When the DECtape controller is set to this mode and the appropriate switches are set in the controller and the transport, the following events take place (see Figure 3-16). The Timing Generator begins to write the timing track and to generate TP00 and TP01. C00 and C01 and MKT count. The WREN flag is set, and the data buffer circuitry starts to shift data into the word buffer. The DF is set, and the correct mark track coding is placed into the data buffer, after which the word buffer is shifted and complemented and the mark track is written (because TM EN H is asserted). The Data Flag (DF) is set every four clock pulses to demand another word, and the DECtape Flag (DTF) is set either with the Data Flag, in normal mode, or after the word count overflows, in continuous mode.

In this way, the timing and mark tracks are written onto a reel of magnetic tape. The codes which must be loaded into the data buffer are explained in Chapter 2. The program which does it is called TOG-8.

3.3.2 Search and Write Data or Write All

Figure 3-17 shows a timing diagram during a search operation which is followed immediately by either a write data or a write all function. During search, the data buffer is continually sampling the data tracks on TP01. As soon as the forward block mark number is detected in the data buffer (at MK BLK MK time), the Data Flag is posted and the number is transferred into the current address register. The computer then switches the controller to WRITE DATA or WRITE ALL mode. In either case, the WR EN (Write Enable) flag is set, the Data Flag (DF) requests a 12-bit word from Memory through the 3-cycle break logic, and writing begins.

The logic shifts a 3-bit word into the word buffer at TP00 time, and it complements this word buffer at TP01 time with the signals SH DTB and COMP + SH H. Simultaneously, the LPB is cleared, and it reads the last two lines of the Reverse PCC Mark cell. The LPB then proceeds to calculate its parity checksum from the data buffer as the writing continues. At the end of the block, the parity register is transferred into the data buffer by the LPB LPB-to-DB signal. This checksum is then written into the first two lines of the PCC Mark cell. If the controller is in Write Data mode, then the data flag does not set again, and the WR EN flag resets. In Write All mode, however, the WR EN flag remains on and the controller requests another data word every four lines.

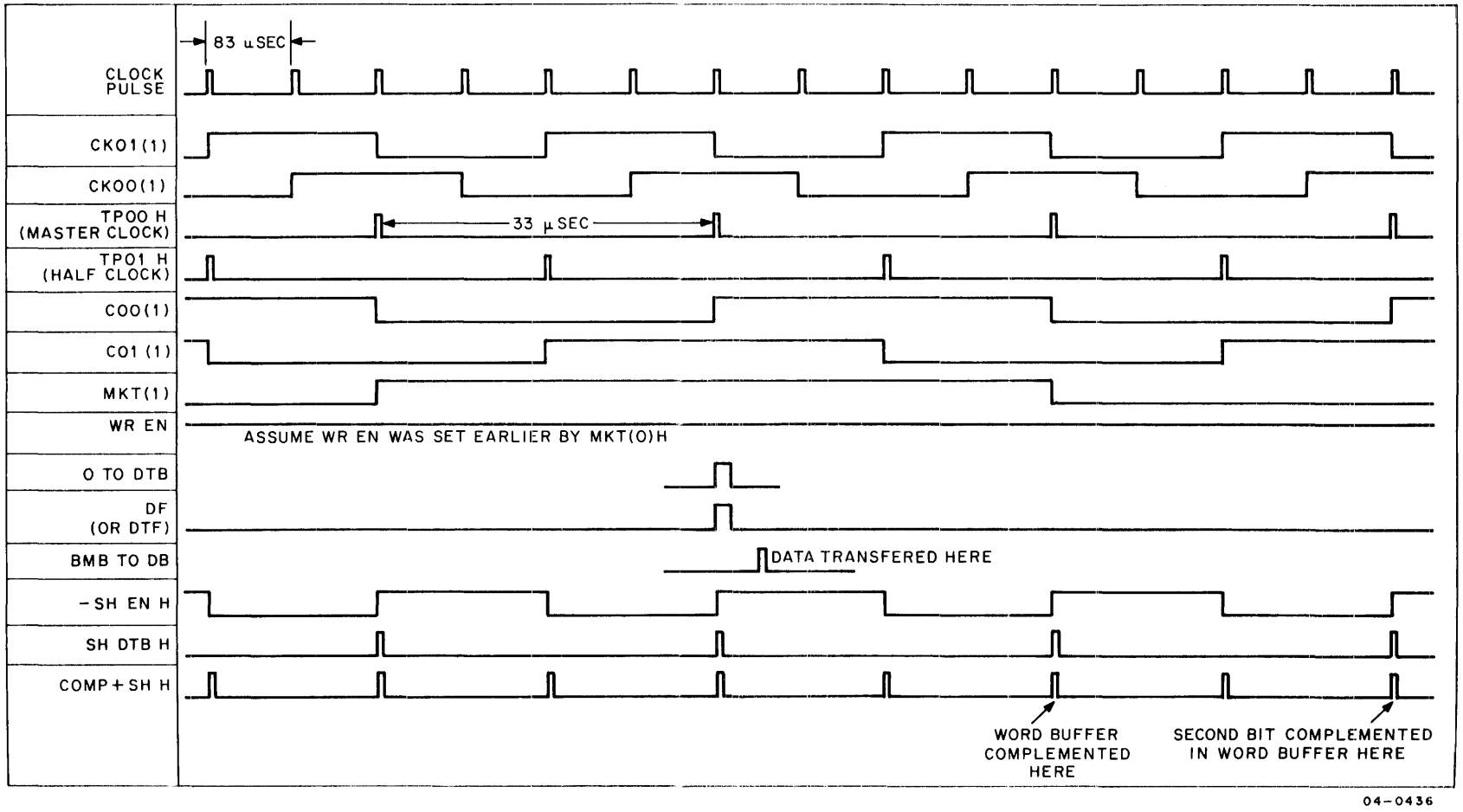


Figure 3-16 Write Timing and Mark Track Timing Diagram

The DECtape flag (DTF) sets with the data flag (DF) during normal search, but only at the end of the word count during continuous search. In Write Data and Write All modes, the DECtape flag (DTF) sets at the end of each block during normal search, but only after the word count overflows during continuous search.

Each of the signals of Figure 3-17 should be examined carefully. Note that a write operation must be preceded by a search operation in order to ensure that the counters are properly synchronized and that the correct block is written into.

3.3.3 Read Data and Read All

Figure 3-18 shows the system timing for the TC08 in Read Data or Read All modes. During these operations, the data buffer and longitudinal parity buffer (LPB) continuously sample the tracks during TP01 times. The Data Flag (DF) is posted as soon as the first 4 lines have passed after the state generator moves into DATA, and every four lines thereafter. The Data Flag stops when ST FINAL is removed during Read Data, but continues during Read All.

At ST CK, the LPB tests to see if it has all ones, and posts a parity error flag if it has not. Parity is not detected during Read All.

3.4 MOVE

The move operation does not cause any significant operation within the controller except to detect the end of tape and post the appropriate error flag. This happens only if that particular tape transport is selected when it runs out of tape. (Note that a tape can be selected, set in motion, then deselected, and it will remember to keep moving.)

3.5 TC08 VERSUS TC08N

As noted in the opening paragraph of Chapter 3, the only difference between the TC08 and the TC08N involves level conversion. The TC08N is designed to be run on the negative logic PDP-8 computer. Modules designed to convert the negative logic to the positive levels available in the controller, and then the reverse, are plugged into the TC08. Prints number TC08-N-11 and TC08-0-1 show these differences.

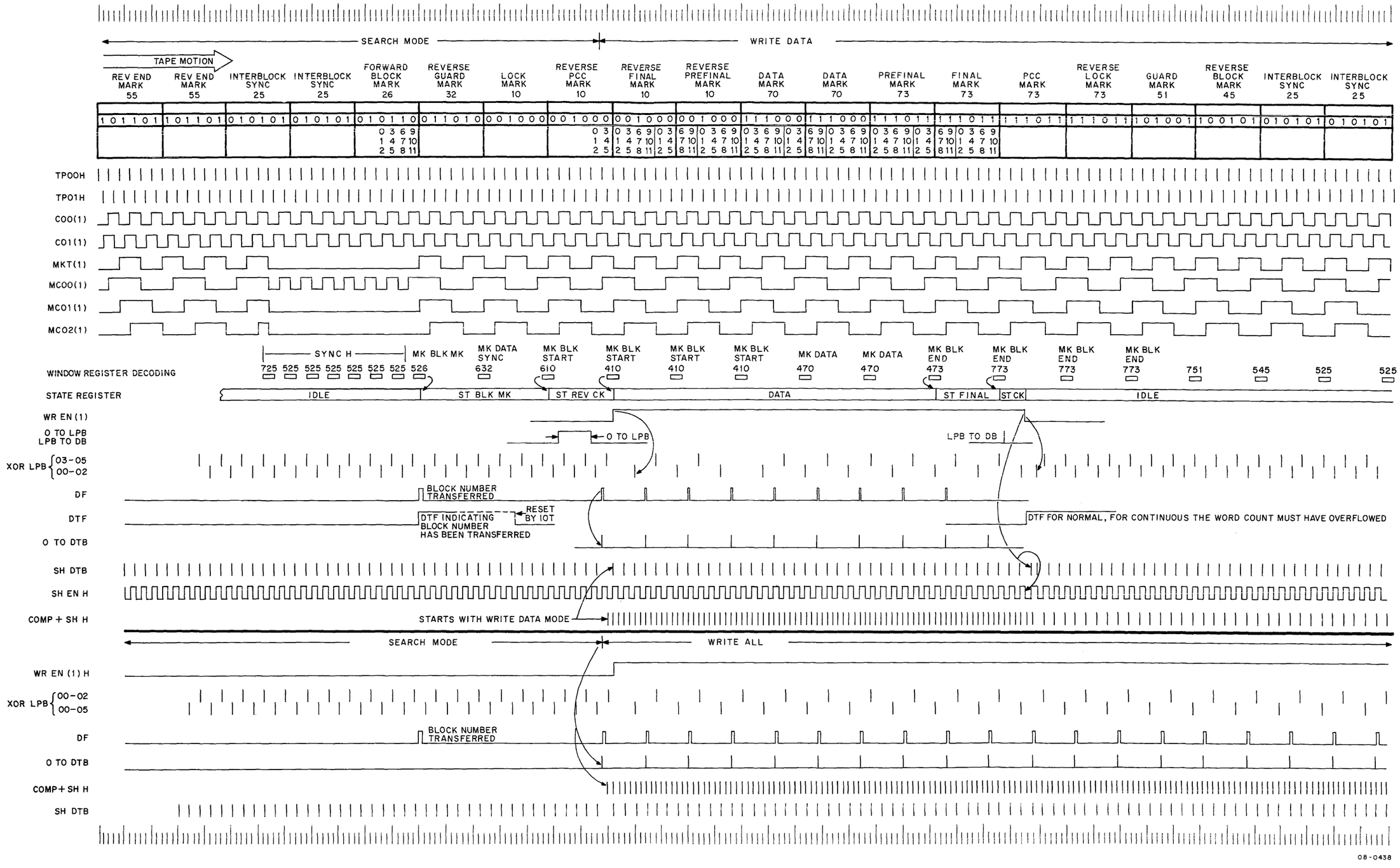
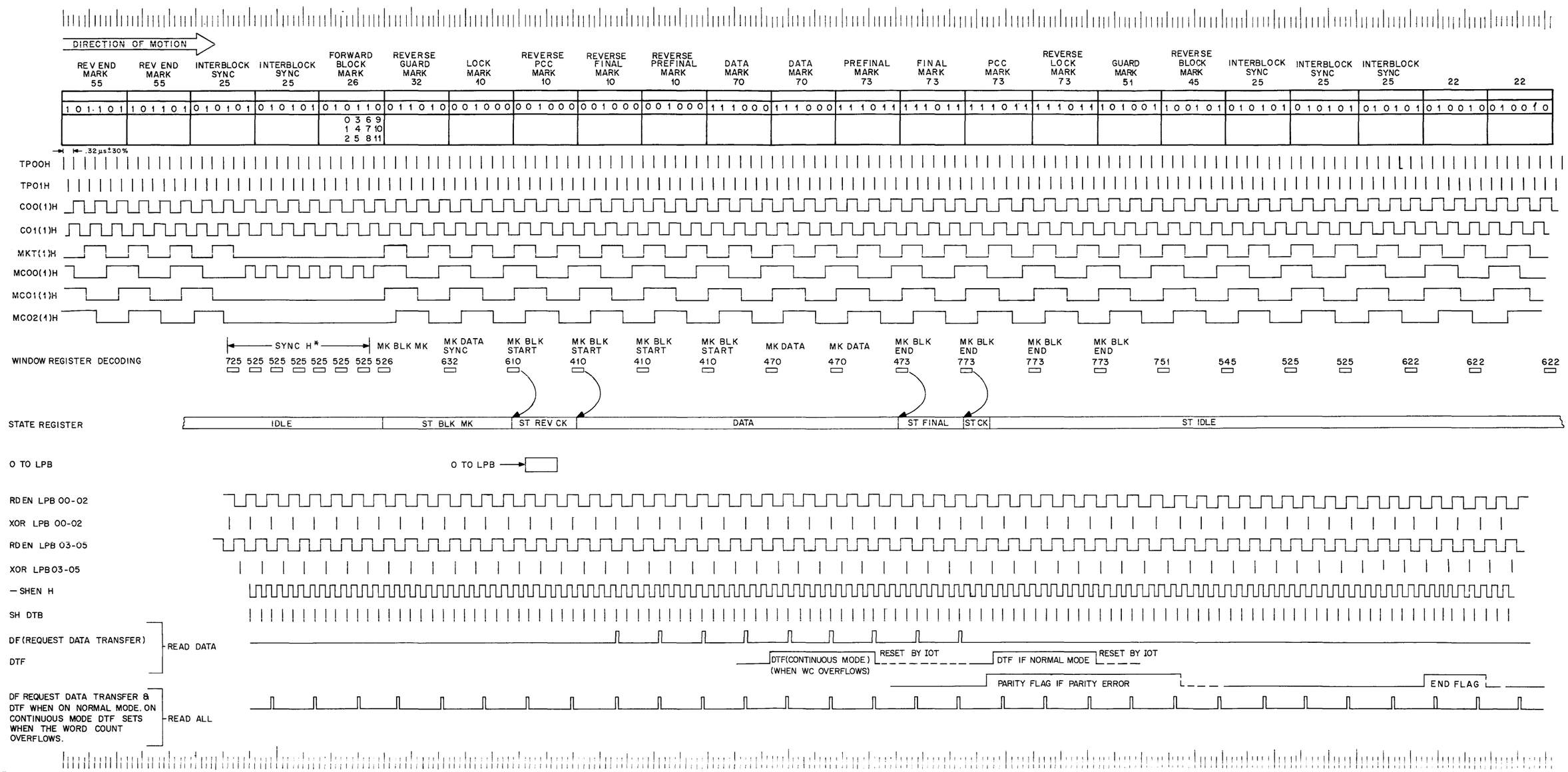


Figure 3-17 Timing Diagram for Driving Search Write Data or Write All



*NOTE: THAT SYNCHRONIZATION OCCURS AT EACH INTERBLOCK SYNC ON READ DATA, BUT ONLY AT THE BEGINING OF THE FIRST BLOCK DURING READ ALL.

08-0437

Figure 3-18 Timing Diagram for Read Data and Read All

CHAPTER 4
INSTALLATION

This chapter provides installation instructions, including unpacking and intercabling instructions, and space, loading, power, and environmental requirements, as well as preliminary checks which should be performed before the equipment is energized and initial turn-on and checkout procedures to ensure that equipment is properly installed.

4.1 UNPACKING

4.1.1 Hardware

Packaging can vary over a wide range, depending on the system configuration ordered by the user. For example, if the user has ordered an entire PDP-8 System, the TC08 is shipped installed in its appropriate rack (see Figure 4-1), together with the required cables. If a whole system is shipped, the interconnecting cables are installed.

If, on the other hand, only a part of a system is shipped because the user already has a programmed data processor, the DECtape system may be shipped separately, but with the cables. Unpack the equipment as follows:

a. Place the equipment package within the installation site near its projected location. Cut the shipping straps and remove all packing material.

b. Open the rear doors, remove the shipping bolts which hold the plenum door closed, and open the plenum door. Remove the machine screw which holds each side of the cabinet to the pallet. Slide the cabinet off the pallet, using a ramp (approximately 4 3/4 inches high) from the floor to the top of the pallet. Move the cabinet to its final location within the installation site.

c. Remove the tape which holds the modules in place within the mounting panels, and the tape which holds the power and interconnecting cables to the floor of the cabinet.

4.1.2 Software

Each DECtape system is shipped with the software required for installation. This diagnostic software includes punched paper tapes, a description of the program, and a listing. Table 4-1 lists the software for the TC08.

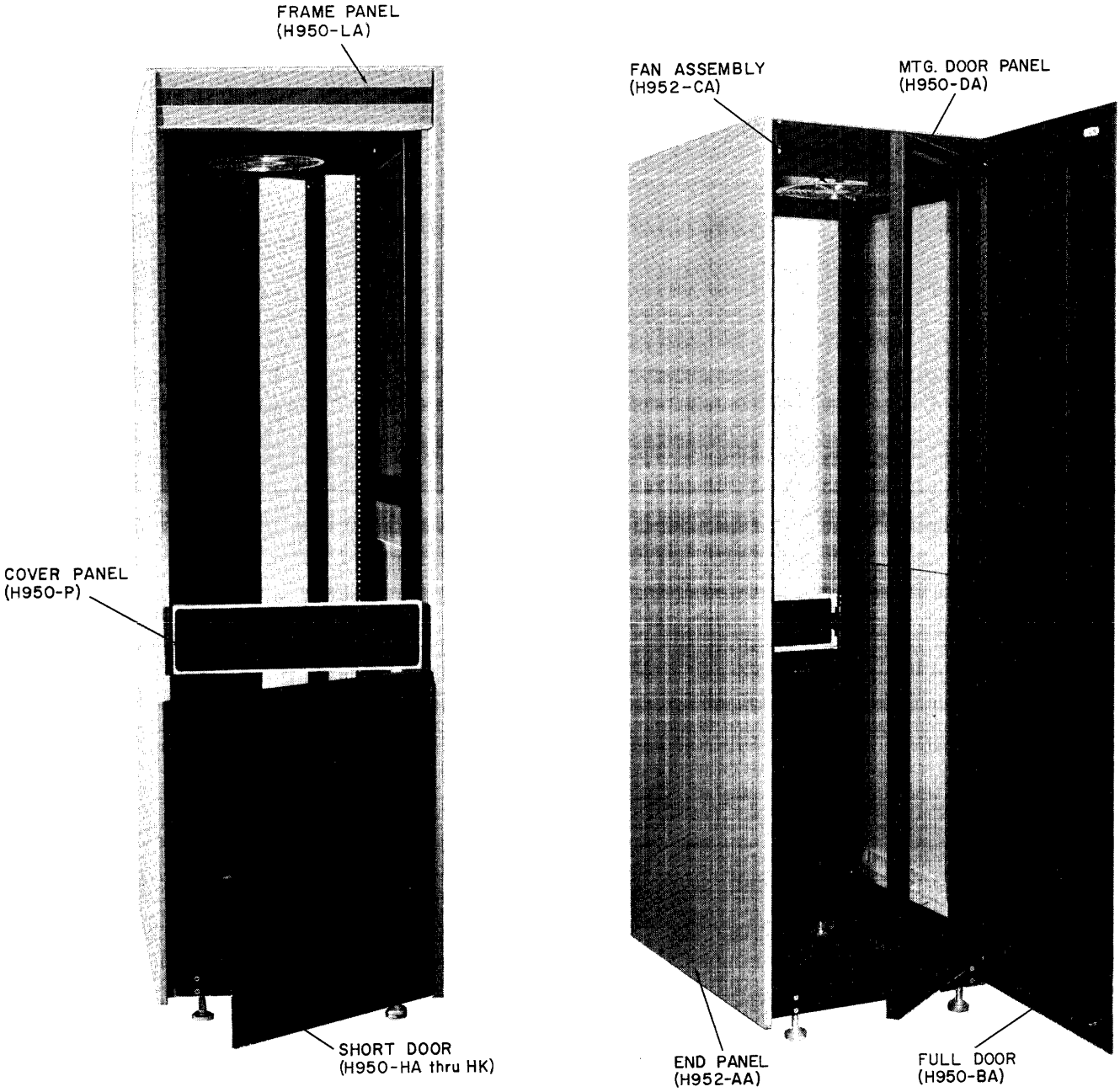


Figure 4-1a H950 Frame

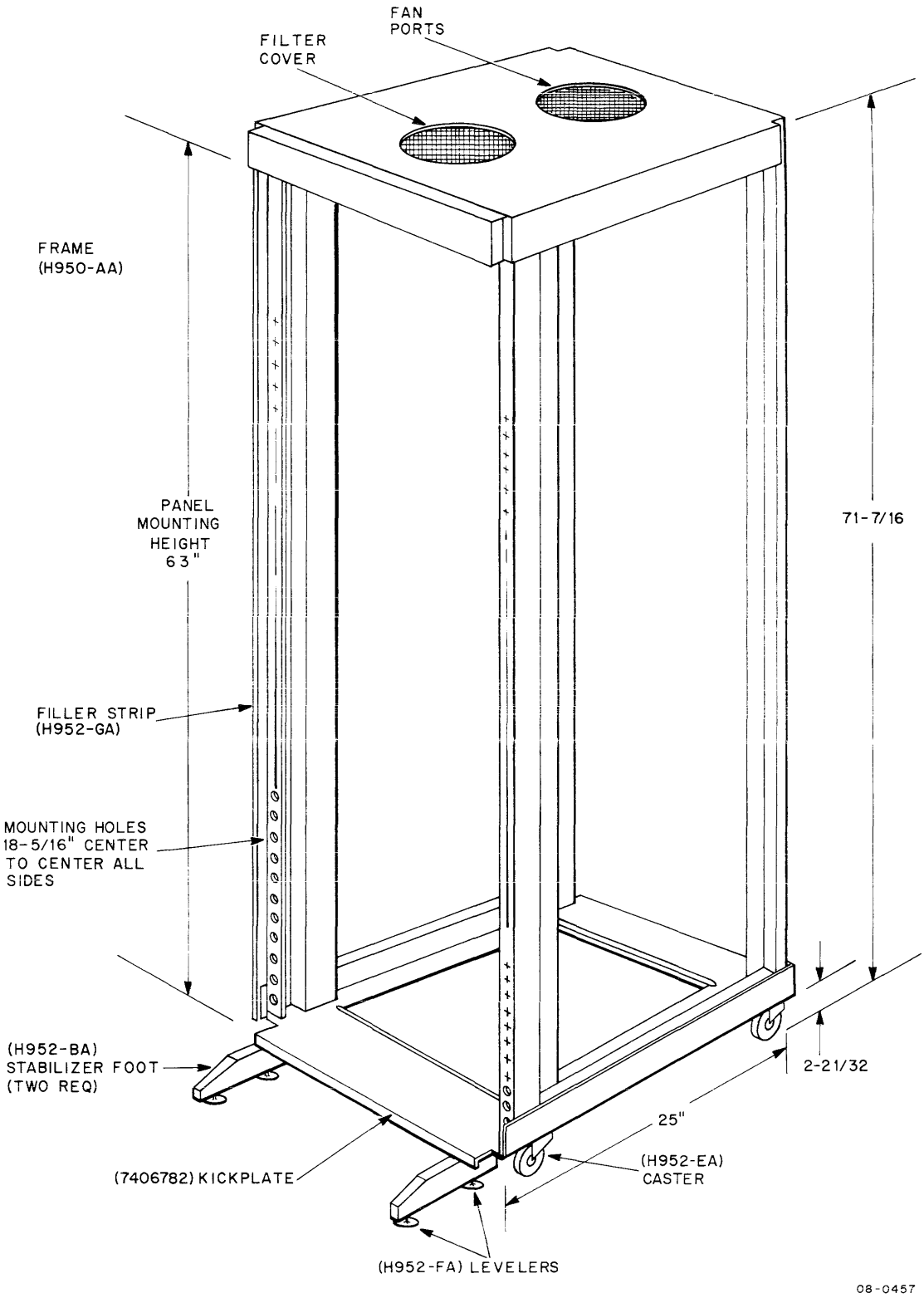


Figure 4-1b H950 Frame, Dimension Diagram

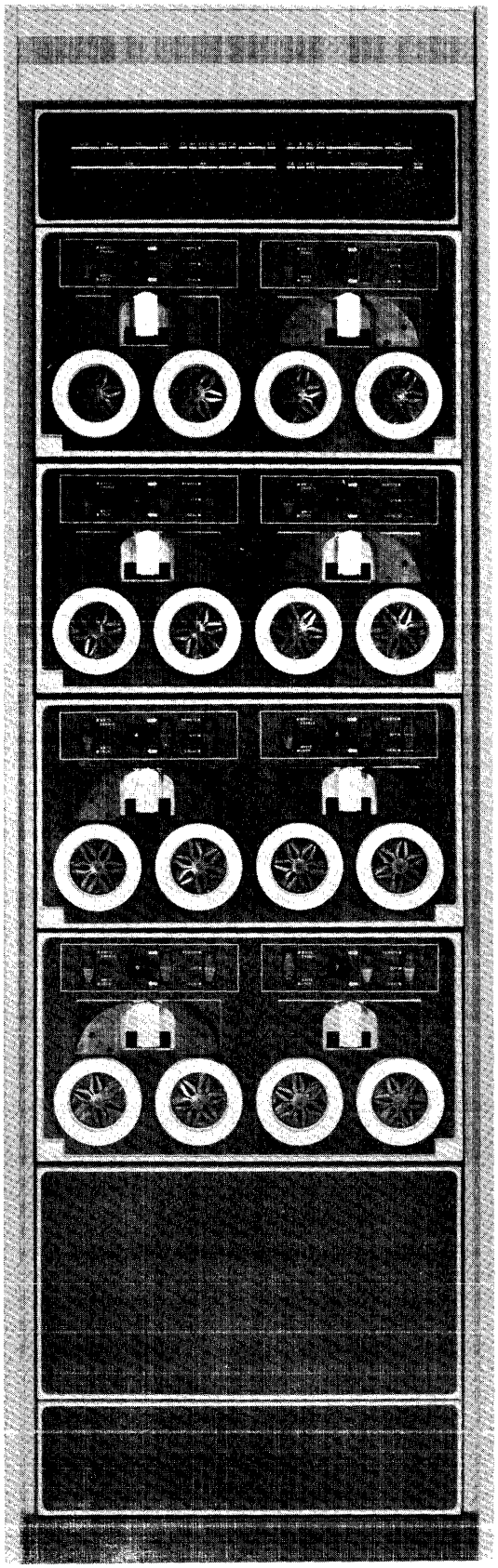


Figure 4-2 DECtape System in Cabinet

Table 4-1
TC08 Software

TC08 BASIC EXERCISER	MAINDEC-08-D3BB-D
TC08 DECTAPE FORMATTER	DEC-08-EUFA-D
TC08 DECTREX 1	MAINDEC-08-D3RA-D
TC08 EXTENDED MEMORY EXERCISER	MAINDEC-08-D3EB-D
TC08 LIBRARY SYSTEM	DEC-08-SUA1-LA

4.1.3 Inspection

Inspect all of the equipment before installing it, checking each piece against the parts list of print TC08-0-15. Table 4-2 lists the cables supplied with a complete system. Any damage must be reported immediately to the shipper and the DEC representative.

Table 4-2
DECtape Cables

Type	Standard Length (Ft)	Number	Use
BC08	8	5	I/O Bus and 3-Cycle Break
W023 - W023	4	1 per TU55 transport	Command Cable
M908 - M908	4	1 per TU56 transport	
W032 - W032	4	1 per transport (TU55 or TU56)	Head Cable
Indicator Cables	5	4	Indicator Panel

4.2 SPACE AND ENVIRONMENTAL REQUIREMENTS

4.2.1 Space Requirements

Figures 4-1 and 4-2 show the clearances required for the DECtape system installed in the PDP-8, 8/I, and 8/L free standing cabinets. When installing the system, be sure that front and rear of the cabinets are accessible to maintenance personnel. If the cabinets are separated by long distances, consideration should be given to overhead trenching ducts or floor ducts for the cabling.

4.2.2 Environmental Requirements

The manufacturer of the magnetic tape recommends that the equipment be operated in a temperature range of 60° to 80°F within 40 to 60% relative humidity.

4.3 POWER REQUIREMENTS

4.3.1 Power Supplies

Power for the operation of the TC08 controller is derived from a standard DEC power supply type 783 or equivalent. The TC08 uses approximately 1/4 of the capacity of the supply. This power can be shared with existing 783 power supplies already installed in the cabinets up to the limits of their respective capacities. The characteristics of the power supply are given in the Logic Handbook. It is designed to mount on the plenum door of the standard 19-inch rack. Power requirements for the TU55 and TU56 transports are given in their respective Maintenance Manuals.

The indicator panel is powered with a 716 Indicator Supply. Its characteristics are summarized in Chapter 6.

4.4 TC08 CABLING

4.4.1 Cabling the TC08 to the Computer

The TC08 should be connected to the PDP-8, 8/I, or 8/L I/O Bus and 3-cycle data break facility. Table 4-3 lists each cable and where it interconnects. All 5 cables are type BC08 bus cables (see Figure 4-3).

Table 4-3
TC08 or TC08N to The PDP-8, 8/I, or 8/L Cabling

I/O Signal Name at TC08	TC08 Location		Location in Computer		
	Out	In	8	8/I	8/L
I/O BAC 00(1)H - I/O BAC 08(1)H	D02	A02	ME34	J01	D36
I/O BAC 09(1)H - I/O PWR CLR H	D02	A02	ME35	J02	D36
I/O BMB 00(1)H - I/O BMB 05(1) H	D03	A03	MF34	J03	D35
I/O BMB 06 (0)H - I/O BMB 11(1)+1	D03	A03	MF35	J04	D35
IM 00 L - IM08L	D04	A04	PE2	J09	D34
IM 09 L - I/O B - RUN(0)L	D04	A04	PE3	J10	D34
DATA 00 - DATA 0 8	D05	A05	PE3	J06	C36
DATA 09 - I/O ADDR ACC 0 H	D05	A05	PF3	J06	C36
DB 00(1)L - DB08(1)L	D06	A06	PE4	J07	C35
DB 09(1) - EA 00 L	D06	A06	PF4	J08	C35

4.4.2 Cabling the TC08 to the TU55 or TU56 Transports

The TC08 is cabled to each of the transports on a 2-cable parallel bus system, shown in Figure 4-3. Table 4-4 summarizes the use and location of each cable.

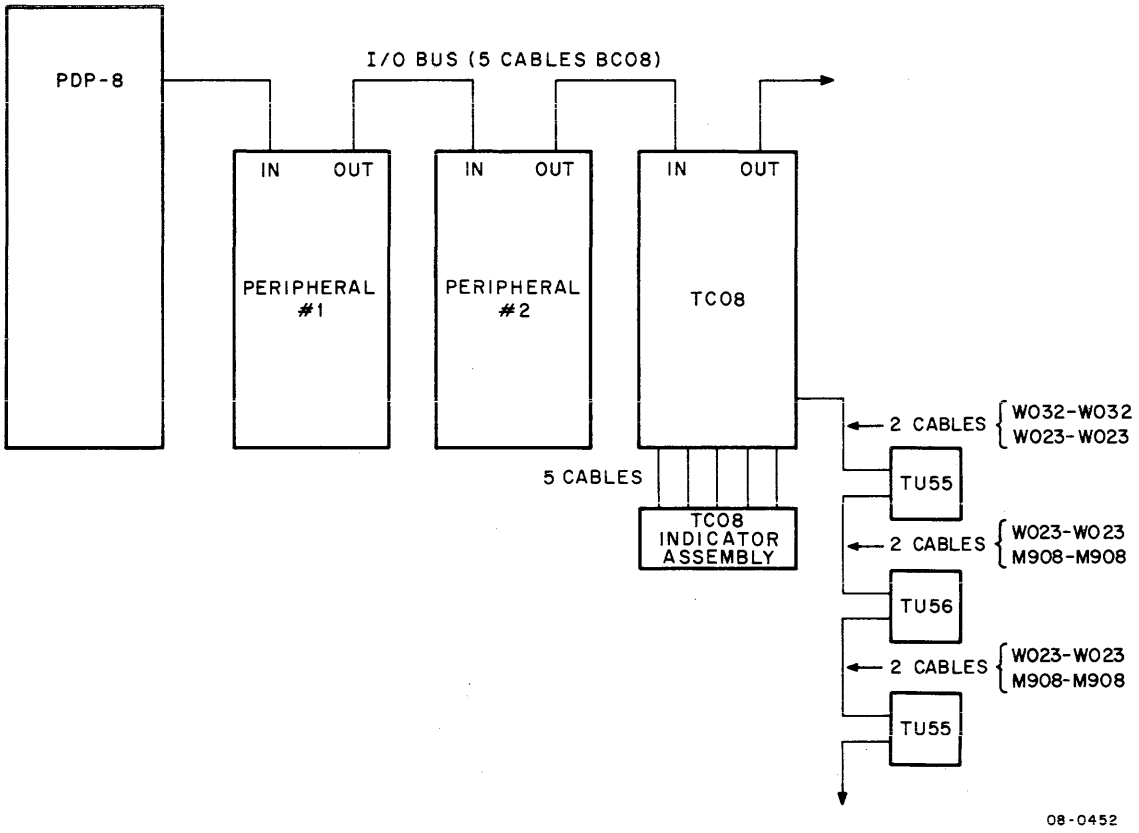


Figure 4-3 DECtape Cables

Table 4-4
Cabling Between the Controller and Transports

Signal Name and Location at TC08	TU55			TU56		
	Cable Type	In	Out	In	Out	Cable Type
TG0 L - T00 L A24	W023-W023	A05	A06	A06	A07	M908-M908
Read/Write Heads A,B19	W032-W032	A,B02	A,B03	A,B10	A,B11	W032-W032

4.4.3 Cabling the Display Panel

Table 4-5 summarizes the signal cabling between the TC08 controller and its display panel.

Table 4-5
Cabling Between the Controller and Display Panel

Signal Names on Indicator Panel	TC08 Location of M916 Connector
USR 0 - MF 0	A25
DTB 0 - LPB 2	A25
MF 1 - MC 2	A26
LPB 3 - WTM	A26

The connectors are M916 boards at the TC08, hard wired into the indicator assembly at the other end. The cables are about 5 feet long.

4.5 FINAL CHECKOUT

After the system is installed, cabled, and powered, it must be made operational. The available tools are the diagnostics, a scope, the logic prints, and the engineer's knowledge of the system.

Final checkout can be approached in one of two ways. The preliminary checks, such as testing for power clear operation, resetting all delays, and checking for the proper operation of each transport, can be done as listed in Chapter 5; or else the field engineer can start directly with the diagnostics. It is recommended that he perform the former, or at least check that all delays are set properly when the diagnostics run. It is important that Chapter 5 be consulted during this period.

CHAPTER 5
CHECKOUT AND MAINTENANCE

This chapter presents the maintenance concept of DECtape, followed by some notes on troubleshooting. The procedures recommended to assemble a TC08 controller are outlined together with TC08 calibration and diagnostics. This chapter assumes that the reader is familiar with Chapters 1 - 4.

5.1 THE TC08 MAINTENANCE CONCEPT

There are only two rules to be followed if the TC08 is to be properly maintained:

1. Carry out the preventive maintenance routines regularly.
2. Always perform a complete checkup on the equipment after troubleshooting a particular fault.

The reasons for the first rule are obvious. Unless cables, wiring, panels, and modules are regularly checked for mechanical problems and unless the heads are free of dirt and the tape is properly handled, even the most reliable tape system will fail.

The reason for the second rule is less obvious. It is important that a DECtape system be completely tested during any troubleshooting because the system is so reliable that borderline faults may not show up until later. Checking all parts of the system may reveal marginal problems that can be repaired immediately. Unless a thorough examination is performed, these faults may occur shortly thereafter, needlessly shortening the mean time between failures on the system.

5.2 TROUBLESHOOTING THE TC08

Everybody has his own style of troubleshooting equipment he knows well. If it is an effective approach, it begins with a thorough check of the most obvious problems; whether the power is on, all cables properly connected, all modules plugged in, and all switches, dials, lights, etc., in their proper state.

The next step is to define the problem, which also involves locating it. Is the computer, the controller, or the transport at fault? Can any one or all be replaced with working equivalents? Usually a system has more than one transport, so that the responsiblility of that unit is easily defined. If the computer is failing, other

peripherals will usually have problems. Once the problems have been located in the controller, a similar procedure should be used to locate the subsystem within the unit (the module) which is at fault. An interesting approach is to record a series of relevant inputs and outputs; then, using the prints and the reading, try to correlate the various symptoms with a possible cause. This usually leads to speculation, more tests, and a solution.

Once the fault is located, the controller should be given a complete examination. All diagnostics should be run, and all delays and the clock properly set up.

The biggest secret to efficient troubleshooting is a thorough knowledge of the machine and of the diagnostics which test it. The TC08 is described in this manual; the diagnostics are described in their respective publications.

5.3 TC08 ASSEMBLY

Before the TC08 is assembled, certain preliminary checks must be performed to avoid damaging the entire unit. These are outlined below. The need for this procedure usually occurs in the factory, although there may be occasions to use it in the field.

5.3.1 Equipment

In order to assemble a TC08 or TC08N control, the following equipment must be available.

a. TC08 back panel
b. TC08 indicator system
c. TC08 or TC08N module kit
d. TC08 and TC08N print set
e. TC08 Maindecs (also called TC01 Maindecs)
f. 738 power supply or equivalent
g. 716 indicator supply
h. A minimum of 1 TU55 or TU56 transport
i. A dual trace scope

5.3.2 Procedure

The procedure for assembling a TC08 or TC08N control is as follows.

a. Inspect the module mounting panel for such mechanical problems as power bus breaks or shorts (usually caused by loose solder or wires), bent or pushed-in pins, broken blocks, and broken wires. Check that the WRTM/NORMAL switch is properly installed.

b. Plug the G821 power regulator card into its slot as shown on the module map of print TC08-0-13. Connect the POWER OK indicator across pins B01 M2 and B01 M1.

c. Connect Power from the 783 power supply to the regulator with the Mate-N-Lock connector. Turn on the 783 and check all power busses in the empty panel. Table 5-1 shows the voltages to check. Turn off the power supply at the end of this test.

Table 5-1
Voltage Test Points

Pins	Correct Voltage
A2	+5V
C2, T1	GND

d. Connect the 716 power supply to the indicator system. Install the indicator cables according to Table 5-2. Turn on power to both the panel and the indicators. All indicators except those which are deliberately tied to ground (i.e., all those without a name) should be ON. If some are not, repair them. Remove all power when this step is completed (see Figure 2-7).

Table 5-2
The Indicator Cables

Signal Name at TC08	TC08 Location	Display Panel Location	Connector Type
USR00(1)H - MF00(1)H	A25	USR0 - MF0	M916 - Hard wired
DTB00(1)H - LPB02(1)H	A25	DTB0 - LPB2	M916 - Hard wired
MF01(1)H - MC02(1)H	A26	MF1 - MC2	M916 - Hard wired
LPB03(1)H - SWTM H	A26	LPB3 - WTM	M916 - Hard wired

e. Plug in the modules according to the module map of print TC08-0-13. Plug in the rest of the cables according to Table 5-3.

Table 5-3
Computer and Transport Cables

I/O Signal Name at TC08	TC08 Location		Location in Computer		
	Out	In	8	8/I	8/L
I/O BAC 00(1)H - I/O BAC 08(1)H	D02	A02	ME34	J01	D36
I/O BAC 09(1)H - I/O PWR CLR H	D02	A02	ME35	J02	D36
I/O BMB 00(1)H - I/O BMB 05(1) H	D03	A03	MF34	J03	D35
I/O BMB 06(0)H - I/O BMB 11(1)+1	D03	A03	MF35	J04	D35
IM 00 L - IM08L	D04	A04	PE2	J09	D34
IM 09 L - I/O B - RUN(0)L	D04	A04	PE3	J10	D34
DATA 00 - DATA 0 8	D05	A05	PE3	J06	C36
DATA 09 - I/O ADDR ACC 0 H	D05	A05	PF3	J06	C36
DB 00 (1)L - DB08(1)L	D06	A06	PE4	J07	C35
DB 09 (1) - EA 00 L	D06	A06	PF4	J08	C35

Signal Name and Location at TC08	TU55		TU56	
	In	Out	In	Out
TGO L - T00 L A24	A05	A06	B04	BJ7
Read/Write Heads A,B19	A,B02	A,B03	A,B10	A,B11

5.4 TC08 PRELIMINARY CHECKOUT AND CALIBRATION

The following steps comprise the procedure for preliminary checkout and calibration of the TC08.

a. Test power clear for correct operation by scoping the power clear input to all flip-flops and turning the computer on and off. A less rigorous test is to check if the indicators go off with power clear.

b. Dial one of the transports to 8 or 0, and any other to different numbers. This is the transport that will be used for the test.

c. To test all the IOTs, key in the following instructions.

Location	Code	Mneumonic
0000	7604	LAS
0001	0010	AND (0017)
0002	1011	TAD (6760)
0003	3005	DCA
0004	1012	TAD (0400)
0005	7402	HLT
0006	5000	JMP START
0007	7402	HLT I/O SKIP
0010	0017	
0011	6760	
0012	0400	

Start the program at location 0000, and set bits 8 - 11 into the switch register to select the IOT code that is to be executed. Table 5-4 shows what the switch register does.

Table 5-4
The Switch Register Bits

Switch Register Bit		State	Code Selector
	8	0	76
	8	1	77
Unselected, these bits do nothing	9	1	IOP4
	10	1	IOP2
	11	1	IOP1

This program executes the IOT instruction that is indicated in the switch register until it is halted. The IOT decoding should be checked by watching the outputs of the M103 decoders with a scope and then placing the correct code and control pulse into the register.

d. Calibrating the TC08 controller involves setting up the various delays. The XSA DY delay shown in print TC08-0-6 can be triggered by placing 0004 into the switch register and starting the preceding IOT program. Set this delay to the value indicated in the prints.

e. To fire the U & M DY delay, shown in Print TC08-0-3, key in the following program. This program causes the direction bit to be XORed at a rate determined by the contents of the switch register. Set the delay to the value shown in the prints.

Start	0000	7604	LAS
	0001	7040	CMA
	0002	3015	DCA
	0003	2014	ISZ
	0004	5003	JMP .-1
	0005	2015	ISZ
	0006	5003	JMP .-3
	0007	1013	TAD
	0010	6764	DTXA
	0011	5000	JMP START

```
0012    7402    HLT I/O SKIP
0013    0400
0014    0000
0015    0000
```

f. Remove the G888 in slot A18 and add a temporary jumper between D14K2 and D14U1: then change address 13 of the previous program to ALL Zeros. The program may be used to fire the SP DY which should be set to the value noted on print TC08-0-3. Set - XTDY also. After these delays are set, remove the jumper, insert the G888 back into slot A18, and replace the original contents of address 13 (0400).

g. Add the following instructions to the previous program, to produce a tape-rocking program. Start this program at location 16.

```
0016    7600    CLA
0017    1023    TAD
0020    6766    DTLA
0021    5000    JMP START
0022    7402    HLT I/O SKIP
0023    0200
```

h. Use the following program to enable and calibrate the write timing and mark track clock.

```
Start   0000    1004    TAD
        0001    6766    DTLA
0002    0002    6764    DTXA
        0003    5002    JMP .-1
        0004    0260
```

Place unit 8 on-line and write enabled. Place WRTM normal switch in the WRTM position. Start the program. The clock should be set to the value noted on engineering drawing D-BS-TC08-0-3.

5.5 TC08 DIAGNOSTIC TESTING

5.5.1 Diagnostics

The controller is now calibrated. The following diagnostics should be run in the order indicated.

a. The TC01 basic exerciser (MAINDEC-08-D3BB-D) or Extended Memory Exerciser (MAINDEC-08-D3EB-D) when applicable.

b. DECtape Formatter (DEC-08-EUFA-D)

c. DECtrex 1 (MAINDEC-08-D3RA-D)

d. The DECtape Library System (DEC-08-SUA1-LA)

e. Elevated temperature testing. The control must run DECtrex 1 for one hour free at 55° Centigrade.

f. Life testing. DECtrex 1 should be run for a minimum of one hour per transport.

5.5.2 Testing the Mark Track Decoder

The most important single subsystem within the controller is the mark track decoder, which is contained within the M228 module. Problems within this module can be the most difficult to diagnose.

a. The following procedure outlines a possible approach. It assumes that the controller can search.

   (1) Load the basic exerciser (MAINDEC-08-D3BB-D) into the computer.

   (2) Have the exerciser rock the tape in search mode.

   (3) Check the output of the mark track reader.

   (4) Check each window flip-flop to see if all are getting set. This can be done by examining the indicator panel or scoping each bit.

   (5) Scope each mark track code. Compare the number of times the code appears against the format.

   (6) The timing pulses are also critical inputs to the mark track decoder. Thoroughly check the timing circuitry.

b. If the machine cannot even search properly, check the following areas of possible fault.

   (1) Are the data flag and the DECtape flag being set properly?

   (2) Is the +1 → CA INH operating during search?

   (3) Are the breaks taking place in the right direction?

   (4) Is the break going to the proper address?

   (5) Is the machine performing a single-cycle break rather than a multi-cycle break?

None of these tips can replace a thorough knowledge of the equipment, and a carefully controlled set of tests.

5.6 DECTAPE PREVENTIVE MAINTENANCE

Preventive maintenance involves visual inspection of the system according to the list in Table 5-5, running the diagnostics, and adhering to the practices listed below.

5.6.1 Handling Magnetic Tape

When tape is handled (during splicing), the operator's hands should be clean to prevent contamination of the tape by body oils and salts. The use of sticky masking tape or cellulose tape as splicing or tail-end hold-down is not recommended, because small deposits of the adhesive will strick to the tape.

Heads and guides should be cleaned regularly to remove accumulations of foreign matter.

Table 5-5
Visual Inspection Checklist

Item	Check
Mechanical Connections	a. Check that all screws are tight and that all mechanical assemblies are secure. b. Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors.
Wiring and Cables	a. Check all wiring and cables for breaks, cuts, frayed leads, or missing lugs. Check wire wraps for broken or missing pins. b. Check that no wire or cables are strained in their normal positions or have severe kinks. Check that cables do not interfere with doors and that they do not chafe when doors are opened and closed.
Air Filters	Check all air filters for cleanliness and for normal air movement through cabinets.
Modules and Components	Check that all modules are properly seated. Look for areas of discoloration on all exposed surfaces. Check all exposed capacitors for signs of discoloration, or leakage, or corrosion. Check power supply capacitors for bulges.
Indicators and Switches	Check all indicators and switches for tightness. Check for cracks, discoloration or other visual defects.

5.6.2 Cleaning DECtape Reels

If the tape is contaminated by dust, carefully wipe the surface and backing of the tape with a lint-free cloth, such as a very soft chamois. Contamination that does not brush off easily can be washed off with a cloth slightly moistened with Freon TF. Aliphatic hydrocarbon-type solvents (heptane, gasoline, naphtha) can also be used, but care should be exercised because they are flammable. Do not use carbon tetrachloride, ethyl alcohol, trichlorethylene, or other unknown cleaning agents because they may soften the oxide, deform the backing, or both.

5.6.3 Storing Tapes

The best method of storage is to place the reel of tape in a self-sealing plastic case supplied for the purpose by DEC, and store it on edge in a storage bin equipped with partitions between each two reels. The plastic case protects tape from dust and sudden changes in humidity and temperature. It also guards both tape and reel from damage in handling when the tape is transported between work and storage areas.

If the tape must be stored in the presence of magnetic fields, either ac or dc, special containers are available which will protect the data from erasure in all but extremely high fields. It is more desirable to store them away from such fields, if at all possible.

Avoid extremes of temperature and humidity. In general, recommended storage conditions are:

Relative humidity:	40 to 60%
Temperature:	60 to 80° F

When extremes in temperature are encountered during storage or transit, tape should be brought to equilibrium before it is used.

5.6.4 Physical Distortion

Most signal dropouts in digital recordings are caused by specks of dust and other contaminants which lift the tape away from the head. However, two other significant causes are dents and creases in the base material. Dents are caused by particles wound up tightly in the roll or by roughness in the surface of the hub on which the tape is wound. These may cause permanent dents or creases in many layers of the tape which cannot be stretched out flat as the tape passes over the head. Stresses in the roll which stretch the backing 5% will usually leave a permanent impression. Stresses below the 5% level are not usually permanent. Creases are caused by handling the tape (i.e., threading, splicing, removing the tape from the guides, etc.) or by damage to the edges of the tape because of uneven winding.

5.6.5 Accidental Erasure or Saturation

The magnetic properties of instrumentation tapes are extremely stable. The magnetic retention is permanent unless altered by magnetic fields such as those generated by permanent magnets or electromagnets. These will probably cause partial erasure if placed within a few inches of the tape.

Both unrecorded and recorded tapes should be kept away from electromagnetic bulk erasers and storage cabinets with magnetic latches. Unrecorded tapes should not be placed near dc magnetic fields, such as traveling-wave-tubes or magetron magnets, because they may become heavily biased or even create gross distortion in the record process (i.e., the resultant signal-to-noise ratio will be reduced).

If parts of the recorder become magnetized, they can cause tape erasure, possible tape saturation, and signal degradation. As a preventive measure, periodic demagnetization of critical parts, particularly heads, is recommended.

5.6.6 Head Care and Head Life

The following factors must be considered when maintaining tape heads.

a. Cleanliness of tape, the transport, and their environment.
b. Maintenance procedures which involve the checking of tape tension, tracking, etc.
c. The abrasiveness of the tape being used.
d. Solvents used for cleaning the heads.

Cleanliness in and around the head area is of utmost importance in all tape machines. Dirt particles become a serious threat to the data "take" because they cause spacing loss. They can also become minute scrapers, gougers, and cutters to the head and tape surfaces when dragged between them.

Care must be taken not to touch the heads with any metallic or hard object to avoid scratching, gouging, or magnetizing the heads. For cleaning the heads, use only alcohol, naptha, Freon TF, or gasoline. Freon TF is probably the best all-around cleaner. It should be noted that most head cleaners will also dissolve lubricating greases and tape binders and should be used carefully, especially around bearings and the tape. Cotton swabs make good disposable cleaning tools.

5.7 MODULE AND ACCESSORY WARRANTIES

The following is a summary of the warranties offered for the TC08 and TC08/N DECtape Controllers.

5.7.1 Type B, R, W, M, K and A Modules

All B, R, W, M, K and A modules shown in Catalog C-105, as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment (providing parts are available). DEC will repair or replace any B, R, W, M, K, or A modules found to be defective in workmanship or material within ten years of shipment for a handling charge of $5.00 or 10% of the list price per unit, whichever is higher. Handling charges will be applicable from one year after delivery.

Notwithstanding anything herein contained to the contrary, the Module Warranty outside the continental U. S. A. and Canada is limited to repair or replacement of the module, and excludes all costs of shipping, customs clearance, or any other related charges.

5.7.2 System Modules

All System Modules, Laboratory Modules, High Current Pulse Equipment, G, S, H, Non-Catalog Flip-Chip Modules and Accessories are warranted against defects in workmanship and material under normal use and service for a period of one year from date of shipment, and DEC will repair or replace any of the above items found to be defective in workmanship or material during that period. Handling charges will be applicable from one year after delivery with the amount of handling charges being available to the purchaser upon request. Notwithstanding anything herein contained to the contrary, the Module Warranty outside the continental U. S. A. and Canada is limited to repair or replacement of the module, and excludes all costs of shipping, customs clearance, or any other related charges.

5.7.3 Shipping

All modules must be returned prepaid to the Digital Equipment Corporation. Transportation charges covering the return of the repaired modules shall be paid by the Digital Equipment Corporation except as required by Paragraphs 5.7.1 and 5.7.2. The Digital Equipment Corporation will select the carrier, but by so doing will not thereby assume any liability in connection with the shipment, nor shall the carrier be in any way construed to be the agent of the Digital Equipment Corporation. Please ship all units to:

Digital Equipment Corporation,
Module Marketing Services - Repair Division,
146 Main Street,
Maynard, Massachusetts 01754

No modules will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization number.

5.7.4 Systems

The TC08 system is warranted against defects in workmanship and material under normal use and service, as discussed below, for a period of three (3) months from the date of installation. Notwithstanding the aforesaid, in the event that DEC is prevented, by causes beyond its control, from properly installing the equipment, the period for this warranty shall be deemed to commence on the thirtieth (30th) day after delivery, or upon installation, whichever is sooner. DEC's sole responsibility under this warranty shall be, at its option, to either repair or replace any component which fails during this period, provided the purchaser has promptly reported same to

DEC in writing and DEC has, upon inspection, found such components to be defective. The purchaser must obtain shipping instructions for the return of any item under this warranty provision. Compliance with such instructions shall be a condition of this warranty.

5.7.5 Other Warranty Conditions

All above warranties are contingent upon proper use in the application for which the products were intended and do not cover products which have been modified without DEC's approval, or which have been subjected to unusual physical or electrical stress, or on which the original identification marks have been removed or altered. These warranties will not apply:

(1) if adjustment, repair, or parts replacement is required because of accident, neglect, misuse, failure of electric power, air conditioning, humidity, control, transportation, or causes other than ordinary use, or

(2) if the equipment is installed by the customer without prior written approval from DEC, or

(3) if the equipment is removed from its location of initial delivery.

5.8 SERVICE POLICY

Unless explicitly agreed upon by the owner and the Digital Equipment Corporation, the responsibility for preventive and corrective maintenance, after the warranties have elapsed, lies solely with the owner of the TC08. Replacement stockpiles, special tools, test equipment, or other auxiliary equipment listed as a requirement for maintenance in this manual, will not be supplied by the Digital Equipment Corporation.

5.9 SPARE PARTS

No spares are shipped with the TC08. Table 5-6, however, lists recommended spares, together with minimum quantities for maintenance. Check the equipment warranty before ordering a spares replacement.

Table 5-6
Recommended TC08, TC08/N Spares

TC08/N		TC08	
Number	Module Type	Number	Module Type
1	G888	1	G888
1	M100	1	M101
1	M102	1	M103
2	M113	2	M113
1	M121	1	M121
2	M206	2	M206
1	M302	1	M302
1	M633	1	M633

Because it is possible to repair modules by replacing faulty components, four of the following chips are recommended for either controller.

DEC 7400 N
DEC 7410 N
DEC 7420 N
DEC 7430 N
DEC 74H40 N
DEC 7474 N

CHAPTER 6

TC08, TC08/N MODULES

This chapter provides descriptions of special modules used in the TC08 or TC08/N controller but not explained in the Logic Handbook. Engineering drawings referred to in this chapter appear in Chapter 7.

6.1 DEC LOGIC

DEC builds three series of compatible below-ground logic (the B-, R-, and S-series), two series of compatible above-ground logic (K- and M-series), an extensive line of modules to interface different types of logic (W-series), a line of special purpose modules (G-series), and a line of support hardware for its module line (H-series).

With few exceptions, the DEC below-ground logic operates with logic levels of ground to -0.3V (upper level) and -3.2V to -3.9V (lower level), using diode gates which draw input current at ground and supply output current at ground. Figure 6-1 shows the voltage spectrum of negative logic systems.

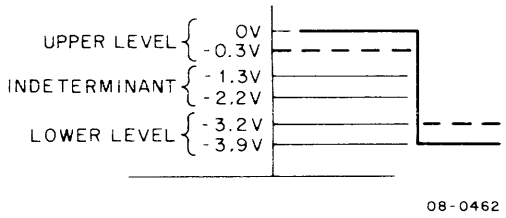


Figure 6-1 Voltage Spectrum of Negative Logic Systems

The compatible above-ground logic generally operates with levels of ground to +0.4V (lower level), and +2.0 to +3.6V (upper level), using TTL or TTL-compatible circuits whose inputs supply current at ground and whose outputs sink current at ground. Figure 6-2 shows the voltage spectrum.

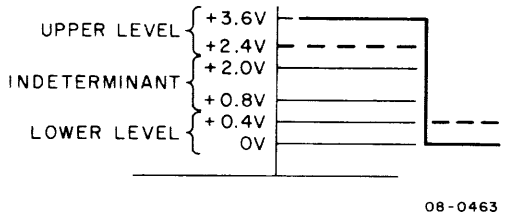


Figure 6-2 Voltage Spectrum of TTL Logic

Finally, a set of special modules designed to operate on the PDP-8 I/O bus are available. Figure 6-3 indicates the voltage spectrum in which they operate.

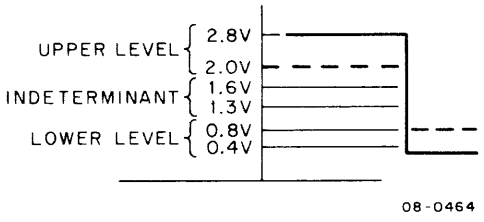


Figure 6-3 Voltage Spectrum for Positive PDP-8 I/O Bus Logic

The DIGITAL Logic Handbook, C-105, is recommended reading for those not already familiar with the basic principles of digital logic and the type of circuits used in DEC logic modules.

6.2 MEASUREMENT DEFINITIONS

Timing is measured with the input driven by a gated pulse amplifier of the series under test, and with the output loaded with gates of the same series, unless otherwise specified. Percentages are assigned as follows: 0% is the initial steady-state level, 100% is the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50% input change to 50% output change. Rise and fall delays for the same module usually are specified separately.

Risetime and falltime are measured from 10% to 90% of waveform change, either rising or falling.

6.3 LOADING

Input loading and output driving are specified in "units", where one unit is 1.6 mA by definition. The inputs to low-speed gates usually draw 1 unit of load. High-speed gates draw 1-1/4 units, or 2 mA.

6.4 MODULE CHARACTERISTICS

6.4.1 G775 Connector Card

This connector card, designed to plug into a standard H911 slot, is used to terminate the 36-wire flexprint cable which interconnects logic signals to the equipment indicator panel. All unused inputs should be grounded. Figure 6-4 shows the logical symbol of the connector card; its circuit schematic appears in Chapter 7 as Engineering Drawing B-CS-G775-0-1.

This connector provides isolation for logic levels so that these levels can directly drive indicator bulbs in the display.

Input loading is 2 units dynamic and 1 unit static (dc).

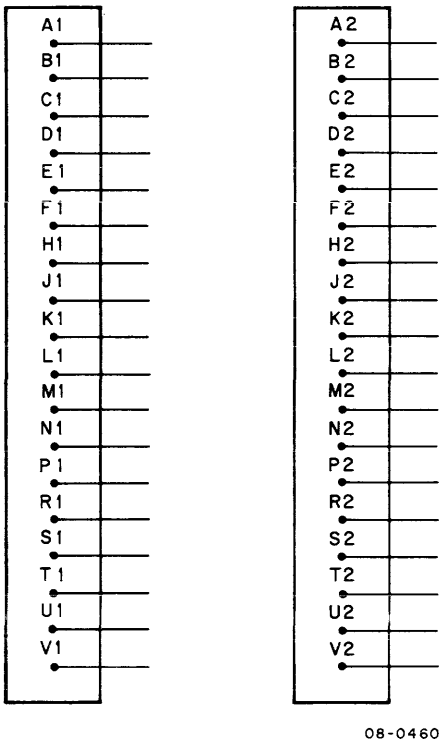


Figure 6-4 The G775 Connector Card Logic Symbol

6.4.2 G879 Transports Detector Module (see Figure 6-5)

This is a series G single-height module designed to detect an error condition in the select circuitry of the DECtape system. It will switch if the input voltage is too low, indicating that no transport has been selected, or too high when more than one has been selected. The circuit schematic appears in Chapter 7 as Engineering Drawing B-CS-G879-0-1.

Inputs: Minimum input impedance 100 Ω

Levels 0V to -15V

Outputs: Standard TTL levels

Fan out - 30 units

Input/Output: Function

Input Voltage	Output Voltage
-15V → -9V	0V
- 9V → -6V	+3V
- 6V → 0V	0V

Power Dissipation: 90 mA from -15V

25 from +5V

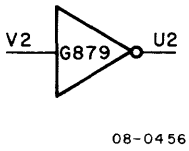


Figure 6-5 The G879 Transport Detector Module

Application: This module was designed to detect when either no transport or more than one transport has been selected in a DECtape system. It can be driven by a W040 module in series with a 100 Ω resistor as shown in Figure 6-6. When either no W040 driver or more than one driver are driving the G879, its output goes negative. With only one input, the output stays high (+3V).

6.4.3 G888 Manchester Reader/Writer Module (see Figure 6-7)

This is a G-series single-height module with a reader and a writer. The reader is a high-gain amplifier with positive feedback which will respond to inputs of 500 μV. There are three stages to the reader; a linear amplifier with a gain of 100, a zero crossing detector, and a limiter which drives a 7400-series TTL gate. A test point, pin M2, is provided to sample the output of the first stage.

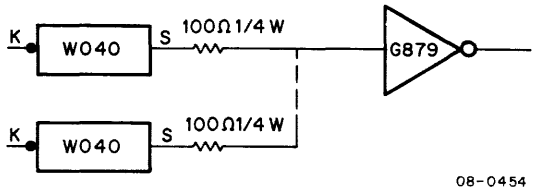


Figure 6-6 G879 Application

The writer is a push/pull amplifier which drives current in one direction or the other as a function of the relative polarity of its inputs. Its inputs feed a 7400-series gate.

Inputs: WRITER

Standard TTL voltage

Load at 0V is 1 unit

R2 should be tied to +3V when not used.

READER

It can detect an input voltage as low as 500 μV.

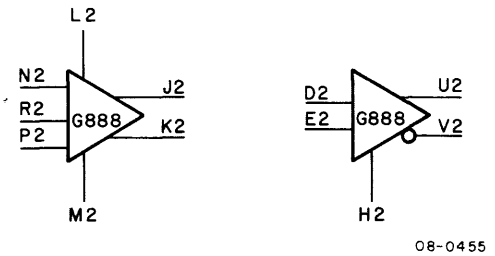


Figure 6-7 The G888 Reader/Writer

Outputs: WRITER

The writer can drive 100 mA in either direction. Pins L2 and M2 are the outputs of the 7400 TTL gates. Pins J2 and K2 are the outputs which drive the tape head.

READER

Outputs U, V are standard TTL voltages.

Fan Out U2 9 units
V2 10 units

Pin H2 is a test point which monitors the output of the first stage.

Standard TTL levels.

Power Dissipation: 50 mW at +5V, 250 mW at -15V. The circuit schematic of the reader/writer appears in Chapter 7 as Engineering Drawing B-CS-G888-0-1.

Application: This module is used to drive or receive current to or from the DECtape heads of the TU55 or TU56 transports.

6.4.4 M100 Bus Data Interface

The M100 is a single-height module which contains fifteen two-input NAND gates arranged for convenient data strobing off the PDP-8 or PDP-8/L negative I/O bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate will be enabled simultaneously. The circuit schematic appears in Chapter 7 as Engineering Drawing C-CS-M100-0-1.

Inputs: Minimum input impedance 5K
Standard negative I/O Bus voltages
Input load at C1 - 15 units

Outputs: Fan Out - 10 units
Input/Output Delay 40 ns typically
Standard TTL levels

Power Dissipation: 10 mA maximum at -15V
60 mA maximum at +5V

Application: The M100 is used to accept data off negative logic PDP-8 buses. It is pin-compatible with the positive logic M101. The enabling line C1 cannot be used as a strobe line because the output signals are indeterminate for 200 ns after the enabling line becomes true. A data input of -3V will yield an output of ground when C1 is gated by a positive voltage level. (See Figure 6-8 for logic diagram.)

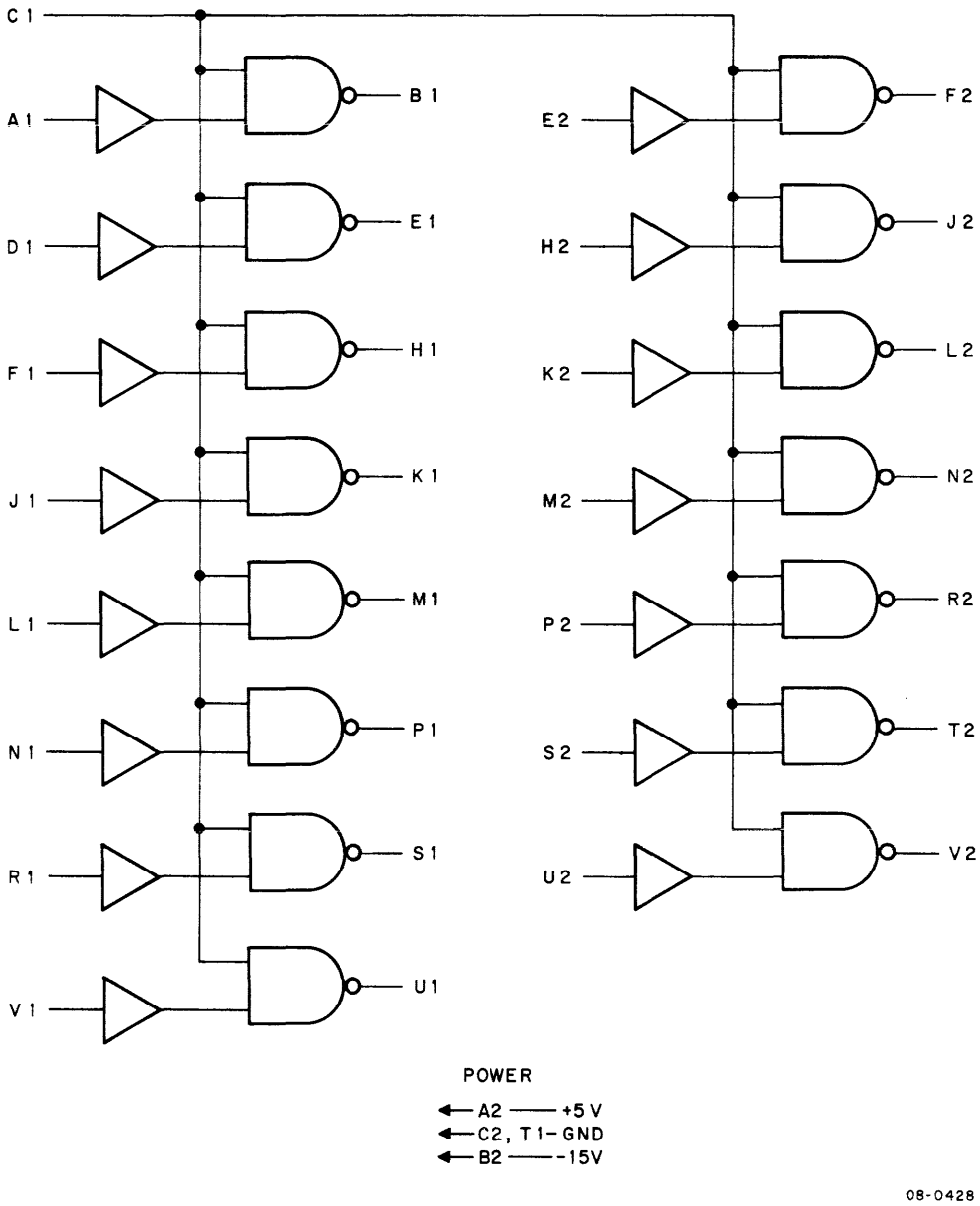


Figure 6-8 The M100 Bus Data Interface Module, Logic Diagram

6.4.5 M102 Device Selector (for use with negative voltage bus)

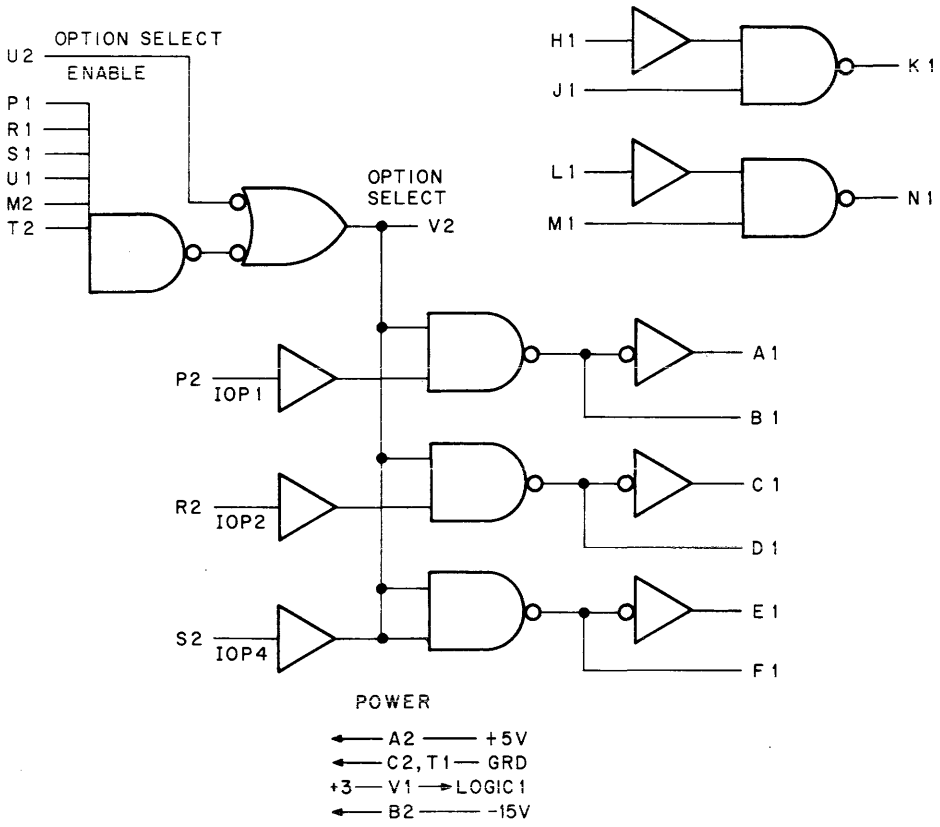


Figure 6-9 The M102 Device Selector

The M102 (see Figure 6-9) is used to decode the six device address bits transmitted in complementary pairs on the negative bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin-compatible with the M103 Positive bus device selector, with the exception of the address inputs. The true states of the BMB outputs of the PDP-8 and PDP-8/I are defined as ground where the true states of the PDP-8/I positive bus and PDP-8/L are defined as an active voltage state. Because of this the complement of the address bits used for an M103 must be connected to the M102.

Because the address complement is tied to the pins D2, E2, F2, H2, J2, K2, an M103 may be directly substituted for an M102 when changing from a negative to a positive bus. The circuit schematic of the M102 appears in Chapter 7 as Engineering Drawing C-CS-M102-0-1.

Inputs: U2 represents 1.25 TTL unit loads, J1, M1 represents 1 TTL P1, R1, S1, U1, M2, and T2 standard levels of -3 volt and ground. Input load is 1 mA, shared among the inputs that are at ground.

P2, R2, S2, H1 and L1
0.2 mA when V in = 0V

0.0 mA when V in = -3V
Propagation Delay 40 ns typ

Outputs: K1 and M1 can drive 10 TTL unit loads. A1, B1, C1, D1, E1, F1 can each drive 37 TTL unit loads. U2 can drive 16 TTL unit loads.

Conversion: Logic Diagram

An active voltage is a True State, i.e., -3V or +3V = "1"

A ground is a True State

Power: +5 V at 130 mA. (maximum).

-15 V at 40 mA. (maximum).

6.4.6 M228 Mark Track Decoder

The M228 mark track decoder is a double-height M-series board designed specifically for the TC08, TC15 DECtape controller. It contains a 9-bit shift register W1-W9, a six-bit state generator, decoding, and control logic. Its operation is explained in detail in Chapter 3 of this manual. The circuit schematic appears in Chapter 7 as Engineering Drawing D-CS-M228-0-1.

Inputs: Standard TTL Voltages	Loading
AV2	26
BH2	18
AS2, BD2, AN2, BR2	1
BC1	12
AR2, BS1, BK2, BL2, BR1	1
AN1	1

Outputs: Standard TTL Voltages	Fan Out
BJ2, BE2, BV2	7
BF2, AK2	8
AL1, AK1, AM2	5
AM1	10
AU1	9
AF1, AH2, BM2, AJ1, AU2, BU1	8
AD2, BT2, BU2	8
AJ2, AT2	6
AF2, BN2, AH1, BP2, BU1, AE2, BS2	10

Power Dissipation: 955 mW at 5V

Application: This module has been designed specifically to perform the mark track decode and state generator functions of the TC08 and TC15 DECtape controller.

6.4.7 W032 Connector

This single-height connector board is intended to be used with 5 cables of 3 conductor shielded coaxial cable. It has no elements. The circuit schematic appears in Chapter 7 as Engineering Drawing B-CS-W032-0-1.

6.4.8 716 Indicator Supply

This power supply delivers 6.5 Vdc and 9 Vac to the indicator panel of the TC08 or TC15 DECtape system. The circuit schematic appears in Chapter 7 as Engineering Drawing B-CS-716-0-1.

Inputs: 115 Vac 50/60 Hz

Outputs: 6.5 Vdc at 4.5A
9 Vac at 100 mA (This is a halfwave rectified signal.)

Power Dissipation: 80W maximum

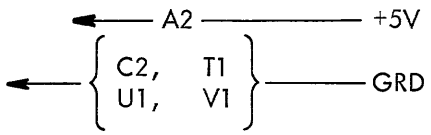
6.4.9 M623 Bus Driver (see Figure 6-10)

The M623 contains twelve two-input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Each driver can sink 100 mA at ground and allows a maximum output voltage of +20V. The output consists of an open collector NPN transistor. The circuit schematic appears in Chapter 7 as Engineering Drawing C-CS-M623-0-1.

Inputs: Input levels are standard TTL levels of 0V and +2.4V. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2, and S2 each present one TTL unit load. All other inputs present two unit loads.

Outputs: A driver output will be at ground when both inputs are at ground. Output rise and fall times of TTL are typically 30 ns when a 100 mA resistive load is connected to a driver output. Output voltage must not exceed +20V.

Power: +5V, 71 mA (maximum) plus external load.



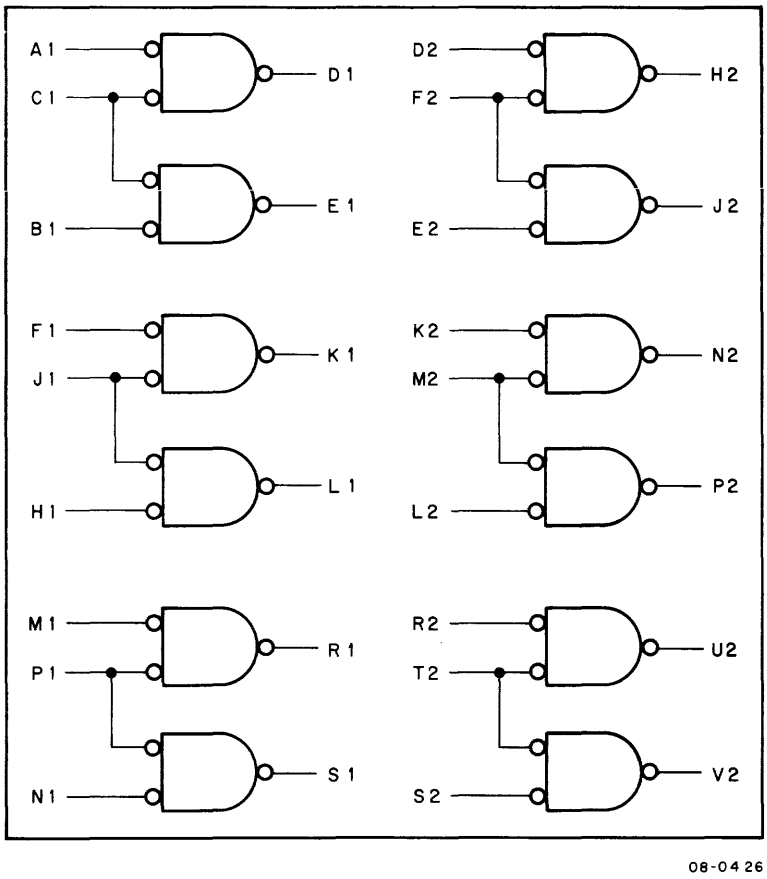


Figure 6-10 M623 Driver

6.4.10 M633 Negative Bus Driver (see Figure 6-11)

The M633 contains twelve bus drivers intended for convenient driving of the negative bus of the PDP-8, PDP-8/I. Each driver consists of an open collector PNP transistor. It is pin-compatible with the M623 positive voltage bus driver. The circuit schematic appears in Chapter 7 as Engineering Drawing C-CS-M633-0-1.

Inputs: Input levels are standard TTL levels. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2, and S2 each present one TTL unit load. All other inputs represent two unit loads.

Outputs: Open collector PNP transistor capable of supplying 20 mA from ground. Voltage applied to the output should not exceed -6V.

Conversion: Logic Diagram: An active voltage is a True State; i.e., -3V or +3V = "1".
A ground is a True State.
Grounded inputs will yield grounded outputs.

Propagation Delay: 40 ns typ

Power: +5V at 100 mA (maximum)
-15V at 40 mA (maximum)

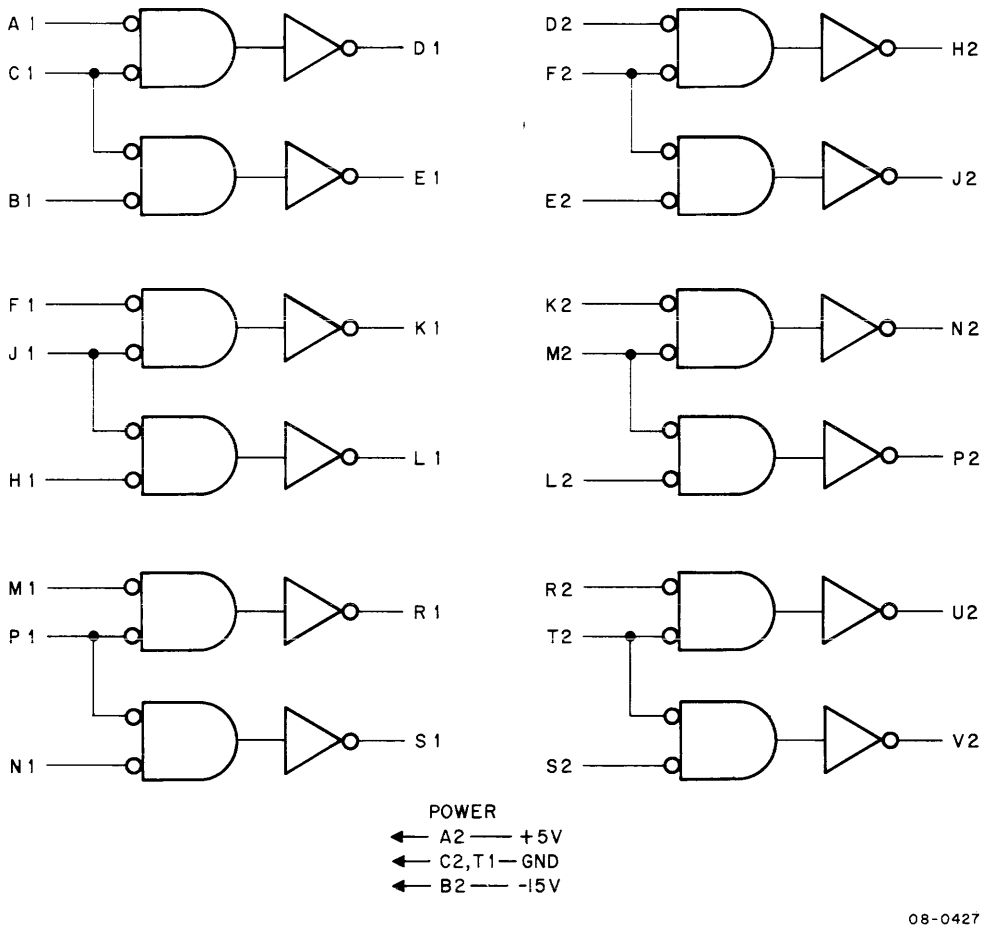


Figure 6-11 M633 Negative Bus Driver

CHAPTER 7
DOCUMENTATION

This chapter contains all of the engineering drawings applicable to this equipment. Table 7-1 lists the signal mnemonics, the full names of the signals, and the prints on which each can be found. The print number in the right-hand column of this table refers to the final digit of the TC08 series of prints; e.g., print 11 would refer to engineering drawing D-BS-TC08-0-11.

These drawings are listed in Table 7-2 by number and title, together with the page in this volume on which each can be found. Because DEC is constantly improving its products, it is possible that several engineering changes might have occurred in the TC08 controller since these drawings were published. In case of discrepancies between the drawings contained in this chapter and those received with the controller, the set of prints which came with the equipment should be used for reference.

Table 7-1
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
0 TO AC	Clear the Accumulator	1, 11
0 TO DTB	Clear the DECtape Buffer	4, 5, 8
0 TO EF	Clear the Error Flags	6
0 TO LPB	Clear the Longitudinal Parity Buffer	9
0 TO STA	Clear the Status A Register	2
0 TO STATE	Clear the State Generator	3, 7
0 TO W	Clear the Window Register	3, 7
1 TO DF	Set the Data Flag	4
1 TO DTF	Set the DECtape Flag	4, 6
ADDR ACC	Address Accepted	1, 4, 11
B - BRK	Break State	1
B - RUN (0)	Computer Not Running	2
B - RUN (1)	Computer is Running	1, 2

Table 7-1 (Cont)
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
B - XSTA	XOR Status Register A Buffered	1, 4, 6
BAC 00 BAC 11	Buffered Accumulator on 0	1, 2, 4, 10, 11
BLK IN SYNC	Block in Synchronization	1, 4
BMB 00 (0) - BMB11 (1)	Buffered Memory Buffer	8, 10, 11
BMB TO DTB	Transfer Memory Buffer to the DECtape Buffer	1, 8
C00 (0), (1)	Counter 0	4, 5, 9, 12
C01 (0), (1)	Counter 1	4, 5, 9, 12
CK00 (0), (1)	Clock Counter 1	3, 10
CK01 (0), (1)	Clock Counter 2	3
CLR DF	Clear Data Flag	4
CLR DTF	Clear DECtape Flag	4
COMP + SH	Complement or Shift	5, 8
CSTA	Clear Status Register A	1, 2, 6
DATA 0, 1	Data State	4, 5, 7, 12
DB00 (0) - DB11 (0)	Data Bits	11, 12
DF (0)	Data Flag on a Zero	4, 5, 11
DF (1)	Data Flag on a One	4, 6, 12
DTB 00 (0) - DTB 11 (1)	Data Buffer 0 - 11	8, 9, 11, 12
DTF (0)	DECtape Flag on a Zero	1, 4, 5, 11
DTF (1)	DECtape Flag on a One	4, 6, 12
DTSF	Skip on DECtape or Error Flags	1
EA 00	Extended Address Bit 0	11, 12
EA 01	Extended Address Bit 1	11, 12
EA 02	Extended Address Bit 2	11, 12
EF (0)	Error Flag on a 0	1, 6, 11
EF (1)	Error Flag on a 1	6, 12
END (0), (1)	End of Tape Error	6, 11, 12
ENI (0), (1)	Enable Interrupt	1, 2, 11, 12

Table 7-1 (Cont)
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
FR 00 (0)	Function Register Bit 0 on a 0	2, 4, 11
FR 00 (1)	Function Register Bit 0 on a 1	2, 4, 12
FR01 (0)	Function Register Bit 1 on a 0	2, 5, 11
FR01 (1)	Function Register Bit 1 on a 1	1, 2, 5, 6, 11, 12
FR02 (0)	Function Register Bit 2 on a 0	2, 11
FR02 (1)	Function Register Bit 2 on a 1	2, 12
FR03 (0)	Function Register Bit 3 on a 0	2, 11
FR03 (1)	Function Register Bit 3 on a 1	2, 12
I/O + 1 TO CA INH	Inhibit Incrementing the CA	11, 12
I/O 0 TO AC	Clear the Accumulator	11, 12
I/O ADDR ACC (0)	Address Accepted	11, 12
I/O B-BRK (0)	Break	1, 12
I/O B - RUN (1)	Computer Running	12
I/O BAC 00 (1) - I/O BAC 11 (1)	Buffered Accumulator	11, 12
I/O BMB 00 (1) - I/O BMB 11 (1)	Buffered Memory Buffer	1, 11, 12
I/O BRK RQ	Break Request	11, 12
I/O BWCO	Buffered Word Count Overflow	11, 12
I/O DATA IN	Data In	11, 12
I/O INT RQ	Interrupt Request	11, 12
I/O PWR CLR	Power Clear	1, 12
I/O SKP RQ	Skip Request	11, 12
I/O TS03	Time State 3	12
I/O TS04	Time State 4	12
IM 00 - 1M11	Input Mixers	11, 12
INT RQ	Interrupt Request	1, 11

Table 7-1 (Cont)
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
IOP 1	Input/Output Pulse 1	1, 12
IOP 2	Input/Output Pulse 2	1, 12
IOP 4	Input/Output Pulse 4	1, 12
LDMF	Load Status Register B	1
LPB 00 (0) - LPB 05 (1)	Longitudinal Parity Buffer	8, 9, 12
LPB NOT EQ 1	Longitudinal Parity Buffer is not Equal to 1	6, 9
LPB TO DTB	Transfer Contents of LPB to the DTB Register	8, 9
M - STOP	Stop the Transport	2, 3
MC 00 (0), (1)	Mark Track Counter Bit 0	4, 5, 6, 12
MC01 (0), (1)	Mark Track Counter Bit 4	4, 5, 6, 12
MC02 (0), (1)	Mark Track Counter Bit 2	4, 5, 9, 12
MF00 (0), (1)	Memory Field Bit 0	1, 11, 12
MF01 (0), (1)	Memory Field Bit 1	1, 11, 12
MF02 (0), (1)	Memory Field Bit 2	1, 11, 12
MK BLK END	Mark Block End	6, 7, 9
MK BLK MK	Mark Block Mark	4, 7
MK BLK START	Mark Block Start	6, 7
MK BLK SYNC	Mark Block Sync	7
MK DATA	Mark Data	6, 7
MK DATA SYNC	Mark Data Sync	7
MK END	Mark End	6, 7
MKT (0), (1)	Mark Track Counter	2, 4, 5, 9, 12
MKTK (0), (1)	Mark Track Head	6, 11, 12
MOVE	Move	2, 6
MR 00 (0), (1) - MR 01 (0), (1)	Motion Register 0, 1	2, 11, 12 2, 3, 11, 12
PAR(0), (1)	Parity Error Flag	6, 11
PC + ES	Power Clear or Error Stop	2, 6
PWR CLR	Power Clear	1, 2, 4, 5, 6
RD + WD	Read or Write Data	2, 4, 6
RD EN	Read Enable	4

Table 7-1 (Cont)
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
RD EN LPB 00-02	Read Enable Longitudinal Parity Buffer Bits 0-2	9
RD EN LPB 03-05	Read Enable Longitudinal Parity Buffer Bits 3-5	9
RDD 00 - RDD 02	Read Data Tracks 0 - 2	8, 9, 10
RDMK (0), (1)	Read Mark Track Head	7, 10
READ ALL	Read All Mode	2, 4
READ DATA	Read Data Mode	2, 4, 6
RSTA	Read Status Register A	1, 11
RSTB	Read Status Register B	1, 11
SE	Select Error Level	2, 6
SEARCH	Search Mode	2, 4, 11
SEL (0), (1)	Select Error	6, 11, 12
SH DTB	Shift the Data Buffer	5, 6, 8
SH EN	Shift Enable	5, 8
SH ST	Shift the State Generator	1, 7
SH ST - B	Shift the State Generator Buffer	1, 7
SHIFT CK	Shift Checksum State	5, 7
SKP RQ	Skip Request	1, 11
SP DY	Speed Delay	3
ST BLK MK (0), (1)	Block Mark State	5, 6, 7, 12
ST CK (0), (1)	Checksum State	4, 5, 6, 7, 12
ST CK 0 P	Checksum State Pulse	4
ST DATA	Data State	5
ST FINAL (0), (1)	Final State	4, 5, 7, 9, 12
ST IDLE (0), (1)	Idle State	5, 6, 7, 9, 12
ST REV CK	Reverse Checksum State	4, 5, 7, 12
SWTM	Write Timing & Mark Track Switch	3, 5, 6, 12
SYNC	Synchronize	4, 7
SYNC - P	Sync Pulse	4
SYNC EN	Enable Synchronization	7
T00	Transport 0	2, 12

Table 7-1 (Cont)
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
T01	Transport 1	2, 12
T02	Transport 2	2, 12
T03	Transport 3	2, 12
T04	Transport 4	2, 12
T05	Transport 5	2, 12
T06	Transport 6	2, 12
T07	Transport 7	2, 12
T FWD	Move Transport Forward	2, 12
T GO	Start the Transport	2, 12
T PWR CLR	Transport Power Clear	2, 12
T REV	Transport Move Reverse	2, 12
T SINGLE UNIT	Transport Single Unit	6, 12
T STOP	Stop the Transport	2, 12
T TRK (0), (1)	Timing Track Head	3, 10
T WRITE OK	Transport Write OK Switch	2, 12
TIM (0), (1)	Timing Error	6, 11, 12
TM EN	Enable Write Timing & Mark	3, 10
TP 00	Timing Pulse 0	3, 4, 5, 6, 7
TP 00 A	Timing Pulse 0 Delayed	3, 5, 9
TP01	Timing Pulse 1	3, 4, 5, 7, 9
TP01A	Timing Pulse 1 Delayed	3, 4, 9
TS03	PDP-8 Timing Pulse 3	1, 11
U + MDY	Unit or Motion Delay	3
USR 00 - USR 02	Unit Select Register	2, 11, 12
UTS (0)	Up to Speed Reset	3
UTS (1)	Up to Speed Set	3, 5, 12
W + UTS	Write Enable or Up to Speed	3
W - INH (0), (1)	Write Inhibit	4, 5
W01(1) - W09(1)	Window Register Bits 1-9	7, 12
WB00 - WB02	Write Buffer	8, 9, 10, 12
WC (0), (1)	Word Count Overflow	1, 4, 5, 12
WCO	Word Count Overflow Pulse	1

Table 7-1 (Cont)
TC08, TC08/N Signals

Signal Mnemonic	Signal Name	TC08 Print
WR EN (0), (1)	Write Enable	3, 5, 9, 10, 12
WRITE ALL	Write All Mode	2, 4, 5
WRITE DATA	Write Data Mode	2, 4, 5
WRITE OK	Write OK	2, 5, 6
WRITE OK + UTS	Write OK or Up to Speed	5
WRTM	Write Timing and Mark Track	2, 3, 5, 6
WRTM + FR03	Write Timing and Mark or Function Register #3	2, 4
XOR TO LPB	Exclusive OR Contents to the Longitudinal Parity Buffer	9
XSA DY	XOR Status A Time Delayed	2, 6
XSAD	XOR Status A Pulse Delayed	1, 6
XSTA	Exclusive OR Status A Register	1, 2, 3, 6
XTDY	Cross Talk Delay	3

Table 7-2
Engineering Drawings

Drawing No.	Title	Page
A-ML-TC08-0	Master Drawing List, DECtape Control	7-9
A-PL-TC08-0-0	DECtape Control	7-10
A-PL-7006394-0-0	Wired Assembly TC08	7-11
A-SP-TC08-0-16	Check-out Procedure (4 Sheets)	7-12
B-CS-G775-0-1	Connector Card Indicator Panel G775	7-16
B-CS-G879-0-1	Transport Detector G879	7-17
B-CS-G888-0-1	Manchester Reader/Writer G888	7-18
B-CS-W032-0-1	Connector W032	7-19
B-CS-716-B-1	Circuit Schematic 716B	7-20
C-CS-M100-0-1	Bus Data Interface M100	7-21
C-CS-M102-0-1	Device Selector M102	7-22
C-CS-M623-0-1	Bus Driver M623	7-23
C-CS-M633-0-1	Negative Bus Driver M633	7-24

Table 7-2 (Cont)
Engineering Drawings

Drawing No.	Title	Page
D-CS-M228-0-1	Mark Track Decoder M228	7-25
D-UA-TC08-0-0	DECtape Control	7-27
D-BS-TC08-0-1	I/O Control	7-29
D-BS-TC08-0-2	Status A	7-31
D-BS-TC08-0-3	TP Generator	7-33
D-BS-TC08-0-4	Flags	7-35
D-BS-TC08-0-5	Control	7-37
D-BS-TC08-0-6	Errors	7-39
D-BS-TC08-0-7	Mark Track Decode	7-41
D-BS-TC08-0-8	DTB/WB	7-43
D-BS-TC08-0-9	LPB	7-45
D-BS-TC08-0-10	I/O Bus Invts/Ind Dvrs	7-47
D-BS-TC08-0-11	I/O Bus Drive Receive	7-49
D-BS-TC08-0-12	I/O Bus Connectors	7-51
D-AD-7006394-0-0	Wired Assembly TC08	7-53
D-DI-TC08-0-15	DECtape Control	7-55
D-TD-TC08-0-17	TC08 Timing	7-57
K-MU-TC08-0-13	Module Utilization List	7-59
K-PL-TC08-0-13	Module Utilization List	7-59
K-WL-TC08-0-14	Wire List TC08	7-60

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MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-TCØ8-Ø-Ø	A	1	DECTAPE CONTROL
A-PL-TCØ8-Ø-Ø	A	1	DECTAPE CONTROL
D-BS-TCØ8-Ø-1	E	1	I/O CONTROL
D-BS-TCØ8-Ø-2	D	1	STATUS "A"
D-BS-TCØ8-Ø-3	C	1	TP GEN
D-BS-TCØ8-Ø-4	B	1	FLAGS
D-BS-TCØ8-Ø-5	A	1	CONTROL
D-BS-TCØ8-Ø-6	B	1	ERRORS
D-BS-TCØ8-Ø-7		1	MARK TRACK DECODE
D-BS-TCØ8-Ø-8	A	1	DTB/WB
D-BS-TCØ8-Ø-9	B	1	LPB
D-BS-TCØ8-Ø-1Ø	A	1	I/O BIS INVTS/IND DVRS
D-BS-TCØ8-Ø-11	C	1	I/O BUS DRIVE/RECEIVE
D-IC-TCØ8-Ø-12	B	1	I/O BUS CONNECTORS
K-(MU,PL)-TCØ8-Ø-13	C	2	MODULE UTILIZATION LIST
K-WL-TCØ8-Ø-14	E	1	WIRE LIST TCØ8
D-AD-7006394-Ø-Ø	A	1	WIRED ASS'Y TCØ8
A-PL-7006394-Ø-Ø	A	1	WIRED ASS'Y TCØ8
D-DI-TCØ8-Ø-15	B	1	DECTAPE CONTROL
A-SP-TC08-0-16	A	1	CHECK-OUT PROCEDURE
D-TD-TC08-0-17		1	TC08 TIMING
D-IC-TC08-0-18	A	1	AC POWER WIRING
D-IC-TC08-0-19	A	1	DC POWER WIRING
D-IC-TC08-0-20		1	CABLE CONFIGURATION
D-AR-TC08-0-21		1	CABINET LAYOUT

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	9/69	00001	D.L.
B	11/69	00002	D.L.
C	12/69	00003	D.L.
D	1/70	00004	D.L.
E	3/70	TC08-5	D.L.
F	4/70	TC08-6	D.L.
H	4/70	TC08-7	D.L.

DRN. G.GIANOULIS	DATE 6/13/69	
CHK'D.	DATE	
ENG.	DATE	
PROJ. ENG.	DATE	
PROD.	DATE 9/2/69	
FIRST USED ON		
SCALE		
SHEET 1 OF 1		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE

DECTAPE CONTROL
60 HZ

SIZE	CODE	NUMBER	REV.
A	ML	TCØ8-Ø	H

DIST.

DEC FORM NO.
DRA 103

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY G. MARINI	CHECKED R. COOK	SECTION
DATE 6/23/69	DATE 7/24/69	
ENG [signature]	PROD [signature]	ISSUED SECT.
DATE [signature]	DATE 9/2/69	

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION TCØ8-060HZ	TCØ8-A50HZ
1	D-AD- 7006331-5-0	INDICATOR PANEL ASSY (TCØ8)	1	1
2	D-AD-7006394-0-0	WIRED ASSY (TCØ8)	1	1
3	1202279	SWITCH, TOGGLE	1	1
4	A-DC-5308493-0-0	DECALS (TCØ8)	1	1
5	9107450-00	WIRE # 24 AWG STRD TEF INS BLK	A/R	A/R
6	9107450-44	WIRE # 24 AWG STRD TEF INS YEL	A/R	A/R
7	D-UA-BCØ8C-Ø-Ø	CABLE, DUAL MYLAR M9Ø3-(2)WØ31	5	5
*	D-UA-832-F-0	POWER CONTROL 832-F	1	
*	D-UA-832-E-0	POWER CONTROL 832-E		1
*	D-UA-783-0-1	783 POWER SUPPLY	1	
*	D-UA-783A-0-1	POWER SUPPLY TYPE 783A		1
*	E-AD-7005474-0-0	FAN ASSY	1	1
*	D-AD-7005909-0-0	AC DIST PANEL	1	1
*	7005128	POWER CORD 25'	1	1
*	1209340-1	Mat-N-LOC CONN	1	1
*	1209378-1	PIN, CONTACT	8	8
*	NOT SHOWN ON ASSY			

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DECTAPE CONTROL	D-UA-TCØ8-Ø-Ø	A	PL	TCØ8-Ø-Ø	A	TC08-00003
	SHEET 1 OF 1	DIST.	G			

DEC FORM NO.
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY G. GIANOULIS DATE 6/12/69	CHECKED CR Carnell DATE 6/27/69	SECTION 1
ENG DATE	PROD DATE T Tarbox 9/2/69	ISSUED SECT. 1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION
1	1205541	BUS STRIP	A/R
2	9107560-1	22 AWG BUS WIRE	A/R
3	9107265-09	#22 TUBING, TEFLON, WHITE	A/R
4	9105740-44	30 AWG SOLID TEF INS. WIRE, YELLOW	A/R
5	9105740-66	30 AWG SOLID TEF INS. WIRE, BLUE	A/R
6	A-DC-7406371-0-0	LOGIC FRAME DECALS	A/R
7	D-AD-5404491-0-0	H911 MTG PANEL	2
REF	K-WL-TCØ8-Ø-14	WIRE LIST TCØ8	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
WIRED ASSY TCØ8	D-AD-7006394-0-0	A	PL	7006394-0-0	A	TC08 00005
	SHEET 1 OF 1	DIST.				

DEC FORM NO.
DRA 11●A

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 9-29-69

TITLE TC08 & TC08N CHECKOUT PROCEDURES

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	———	TC08-00005	LAZUKA	3-27-70	E. T.	4-14-70

A. EQUIPMENT REQUIREMENTS

1. TC08 Back Panel
2. TC08 Indicator System
3. TC08 or TC08N Module Kit
4. TC08 and TC08N Logic Prints
5. Set of TC01 Maindec's
6. 783 Power Supply or Equivalent
7. 716 Indicator Supply
8. Minimum of 1 TU55 or TU56 Transport
9. Dual Trace Scope

B. PRELIMINARY CHECKS

1. With all other modules removed, plug in the G821 power regulator and connect the power OK indicator across pins BØ1M2 and BØ1M2.

2. Inspect panel for discrepancies such as power bus shorts, broken module blocks, broken wires, bent or pushed in pins, and correct installation of the WRTM - normal switch.

3. By using a Mate-N-Lok connector, connect power to the regulator and apply power to the empty panel and check power bus for correct voltage.

4. Connect the 716 power supply to the indicator system and install cables. Power up the empty logic panel and the indicator system. All indicators except those that are deliberately tied to ground should be ON.

C. PRELIMINARY CHECKS AND SETUP

1. Plug in all modules and cables.

2. Test power clear for correct operation.

ENG	APPD	SIZE	CODE	NUMBER	REV
D. Lazuka		A	SP	TC08-0-16	A

DEC FORM NO.
DRA 107A

3. Key in the following instructions:

LOCATION	CODE	MNEUMONIC
ØØØØ	76Ø4	LAS
ØØØ1	ØØ1Ø	AND (ØØ17)
ØØØ2	1Ø11	TAD (676Ø)
ØØØ3	3ØØ5	DCA
ØØØ4	1Ø12	TAD (Ø4ØØ)
ØØØ5	74Ø2	HLT
ØØØ6	5ØØØ	JMP START
ØØØ7	74Ø2	HLT I/O SKIP
ØØ1Ø	ØØ17	
ØØ11	676Ø	
ØØ12	Ø4ØØ	

This program will execute IOT instructions to device 76 or 77 IOPS 1, 2, or 4 under control of AC switch bits 8-11.

4. The IOT decoding should not be tested. By watching the outputs of the IOT decoders with a scope and placing the IOP in the switch register.

5. Place ØØØ4 in the switch and set the XSA DY to the value noted on the prints.

6. Key in the following program:

Start	ØØØØ	76Ø4	LAS
	ØØØ1	7Ø4Ø	CMA
	ØØØ2	3Ø15	DCA
	ØØØ3	2Ø14	ISZ
	ØØØ4	5ØØ3	JMP .-1
	ØØØ5	2Ø15	ISZ
	ØØØ6	5ØØ3	JMP .-3
	ØØØ7	1Ø13	TAD
	ØØ1Ø	6764	DTXA
	ØØ11	5ØØØ	JMP (START)
	ØØ12	74Ø2	HLT I/O SKIP
	ØØ13	Ø4ØØ	
	ØØ14	ØØØØ	
	ØØ15	ØØØØ	

This program causes the direction bit to X ORed at a rate determined by the contents of the switch register. This program generates U&M and also fires the U&M DY which should now be set to the value noted on the prints.

7. By removing the G888 in slot A18 and adding a temporary jumper between D14K2 and D14U1, and also changing address 13 of the previous program to ALL ZERO's!! The program may be used to fire the SP DY which should now be set to the value noted on the prints. After the SP DY is set, remove the jumper, insert the G888 back into slot A18, and replace the original contents of address 13 (Ø4ØØ).

8. By adding the following instructions to the previous program, a tape rocking program can be produced. Start program at location 16.

```
ØØ16   76ØØ      CLA
ØØ17   1Ø23      TAD
ØØ2Ø   6766       DTLA
ØØ21   5ØØØ      JMP START
ØØ22   74Ø2       HLT I/O SKIP
ØØ23   Ø2ØØ
```

9. By using the following program the write timing and mark track clock may be enabled:

```
Start  ØØØØ      1ØØ4      TAD
       ØØØ1       6766      DTLA
       ØØØ2       6764      DTXA
       ØØØ3       5ØØ2      JMP .-1
       ØØØ4       Ø26Ø
```

Place unit 8 on-line and write enabled. Place WRTM normal switch in the WRTM position. Start the program. The clock should be set to the valve noted on the prints.

D. BASIC TESTING

1. The TC01 basic exerciser (Maindec-08-D3BB-D) provides a comprehensive test procedure. The tests also follow in a logical sequence of testing. If this sequence is followed, checkout time and problems will be held to a minimum.

2. After all tests of the basic exerciser have been run correctly, the DECtape formatter (DEC-08-EUFA-D) should be run.

3. DECtrex 1 (Maindec-08-D3RA-D) should be made to run error free.

4. The DECtape Library System (DEC-08-SUA1-LA) should now be tried. And made to run correctly.

E. ELEVATED TEMPERATURE TESTING

1. The control must run DECtrex 1 for ONE hour error free at 55° centigrade.

F. LIFE TESTING

1. With all of the transports being shipped with the system, DECtrex 1 should be run for a minimum of ONE hour per transport.

G. CLEANUP AND ADDITIONAL TESTS

1. Checkout of the control is now complete.

2. Most DECtape systems are shipped in a cabinet and the system must be run after its installation in the cabinet before acceptance.

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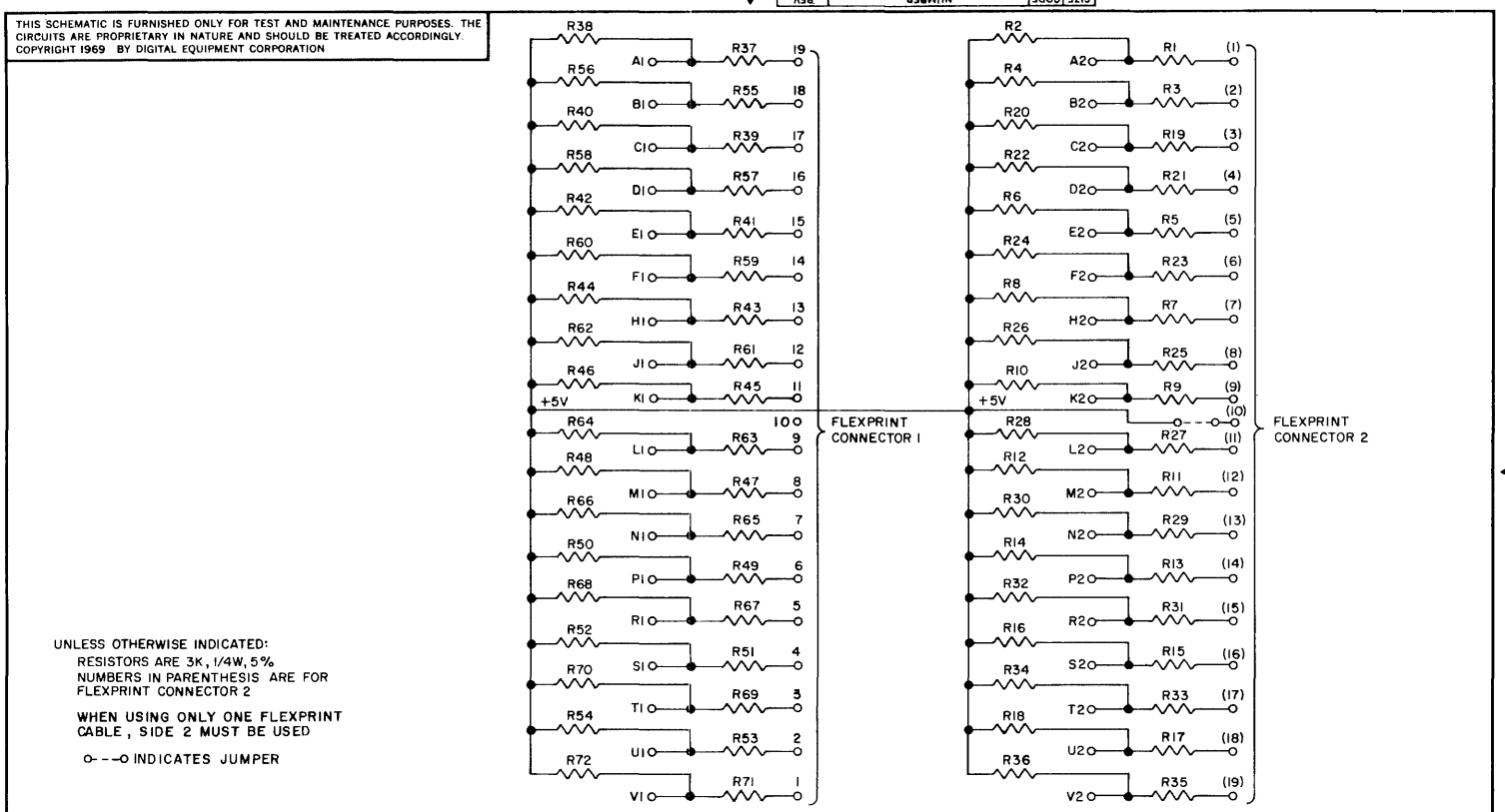

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 3K, 1/4W, 5%
NUMBERS IN PARENTHESIS ARE FOR FLEXPRINT CONNECTOR 2

WHEN USING ONLY ONE FLEXPRINT CABLE, SIDE 2 MUST BE USED

o- - -o INDICATES JUMPER

REVISIONS	CHK	CHG NO	REV
	PL	00001	B
		00002	C

DRN. BUTLER	DATE	5/28/69
CHK'D	DATE	6/16/69
ENG	DATE	9/17/69
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE CONNECTOR CARD INDICATOR PANEL G775

SIZE	CODE	NUMBER	REV.
B	CS	G775-0-1	C

PRINTED CIRCUIT REV. A B C

DEC FORM NO. DRB 102

5

DIST 329, 429, 435 PINK

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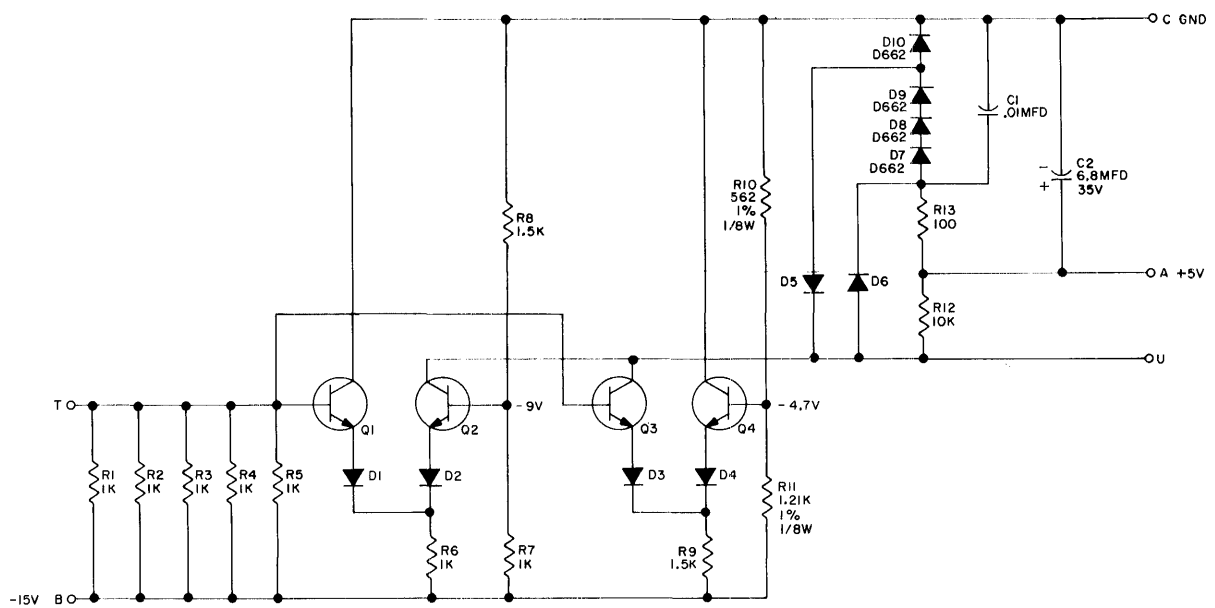


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
DIODES ARE D664
TRANSISTORS ARE DEC3009B

REVISIONS		
CHK	CHG NO	REV.

DRN. BUTLER	DATE 7/2/69	
CHK'D G. Yanga	DATE 7/7/69	
ENG. D. Zgubin	DATE 7/3/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	1N3606		
D662	1N645		
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

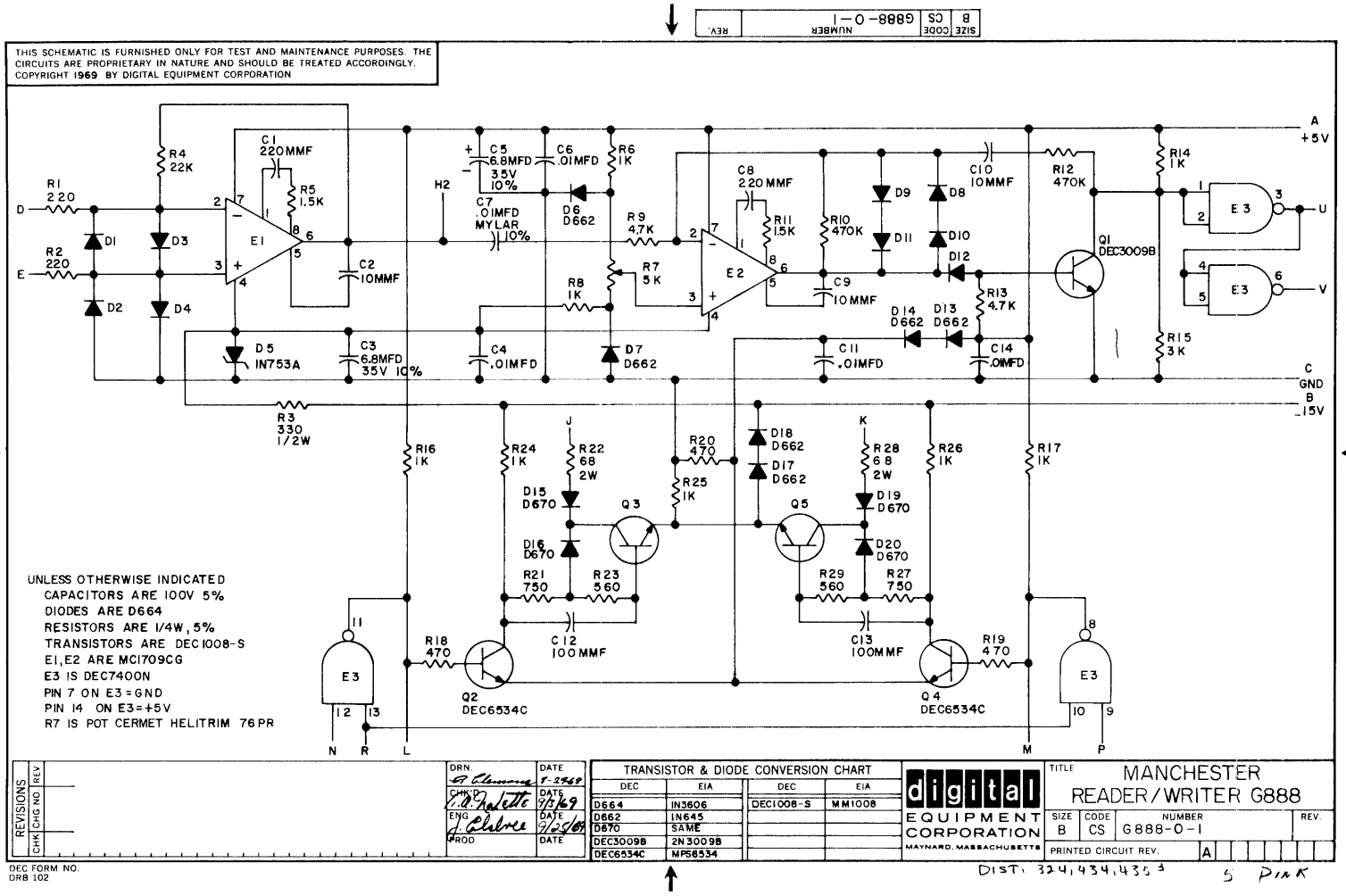
TITLE TRANSPORT DETECTOR G879

SIZE	CODE	NUMBER	REV.
B	CS	G879-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRB 102

5 DIST. 324, 434, 433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UNLESS OTHERWISE INDICATED
CAPACITORS ARE 100V 5%
DIODES ARE D664
RESISTORS ARE 1/4W, 5%
TRANSISTORS ARE DEC1008-S
E1,E2 ARE MC1709CG
E3 IS DEC7400N
PIN 7 ON E3=GND
PIN 14 ON E3=+5V
R7 IS POT CERMET HELITRIM 76PR
A +5V
C GND
B -15V
D
E
U
V
N
R
L
M
P
E1
E2
E3
Q1 DEC3009B
Q2 DEC6534C
Q3
Q4 DEC6534C
Q5
R1 220
R2 220
R3 330 1/2W
R4 22K
R5 1.5K
R6 1K
R7 5K
R8 1K
R9 4.7K
R10 470K
R11 1.5K
R12 470K
R13 4.7K
R14 1K
R15 3K
R16 1K
R17 1K
R18 470
R19 470
R20 470
R21 750
R22 68 2W
R23 560
R24 1K
R25 1K
R26 1K
R27 750
R28 68 2W
R29 560
C1 220MMF
C2 10MMF
C3 6.8MFD 35V 10%
C4 .01MFD
C5 6.8MFD 35V 10%
C6 .01MFD
C7 .01MFD MYLAR 10%
C8 220MMF
C9 10MMF
C10 10MMF
C11 .01MFD
C12 100MMF
C13 100MMF
C14 .01MFD
D1
D2
D3
D4
D5 IN753A
D6 D662
D7 D662
D8
D9
D10
D11
D12
D13 D662
D14 D662
D15 D670
D16 D670
D17 D662
D18 D662
D19 D670
D20 D670
H2
J
K
REVISIONS
CHK
CHG NO
REV
DRN.
DATE
CHK'D
DATE
ENG.
DATE
PROD
DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
D664 IN3606
D662 IN645
D670 SAME
DEC3009B 2N3009B
DEC6534C MPS6534
DEC1008-S MM1008
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
MANCHESTER READER/WRITER G888
SIZE B
CODE CS
NUMBER G888-0-1
REV.
PRINTED CIRCUIT REV.
A
DEC FORM NO. DRB 102
DIST. 324,434,435 3
5 PINK

SIZE	CODE	NUMBER	REV.
B	CS	W032-0-1	

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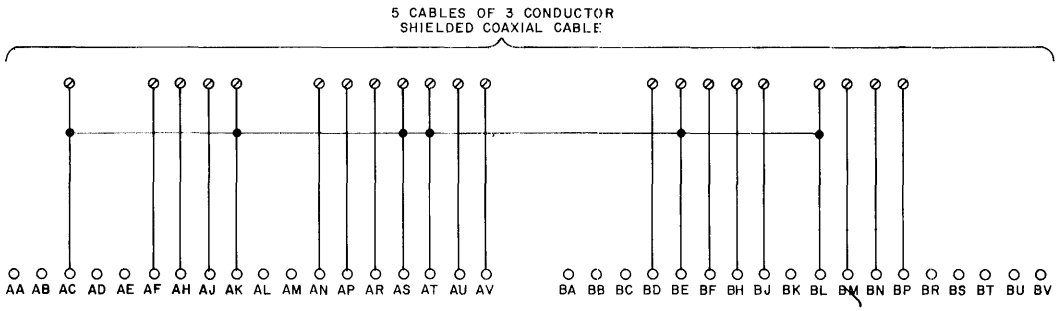

NOTE:
Ø ARE SPLIT LUGS

PARTS LIST IS A-PL-W032-0-0

REVISIONS	REV.	CHG NO.	CHK

DRN.	M. Keller	DATE 10-16-68
CHK'D	[illegible]	DATE 10-17-68
ENG	[illegible]	DATE 11-12-68
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: CONNECTOR W032

SIZE	CODE	NUMBER	REV.
B	CS	W032-0-1	

PRINTED CIRCUIT REV. A

DIST | 434 | 1135 | 359 | PINK

DEC FORM NO
DRB 102

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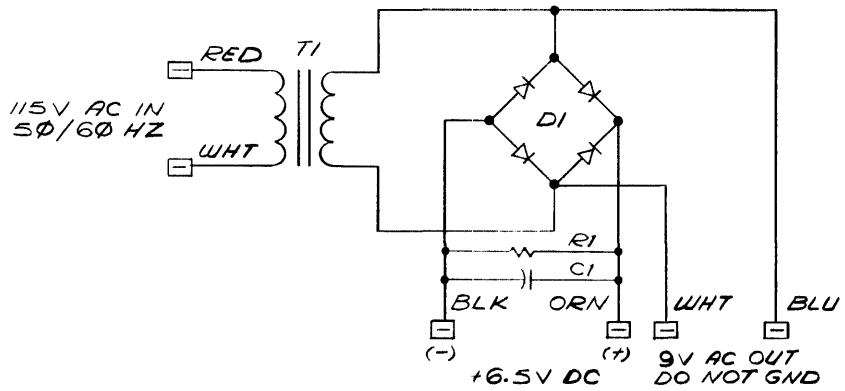

REF DESIGNATION	DESCRIPTION	PART NO
C1	CAP 18,000 MFD 10V DC	1009437
R1	RES 5 Ω 25W, W.L.	1300165
	PARTS LIST	D-UA-716-B-Ø
T1	XMFR#F64-U TRIAD	1609588
D1	DIODE PACK DM-2	1105392

PARTS LIST

FIRST USED ON OPTION/MODEL: 716-B

REVISIONS			
CHK	CHG NO.	REV	

DRN	Robichaud	DATE 10-9-69
CHK'D	D. Healy	DATE 10-28-69
ENG	J. Zel	DATE 1-5-70
PROD	G. Bundy	DATE 1-6-70

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: CIRCUIT SCHEMATIC 716B

SIZE	CODE	NUMBER	REV
B	CS	716-B-1	

PRINTED CIRCUIT REV.

DEC FORM NO. DRB 102

SIZE B CODE CS 716-B-1 NUMBER REV.

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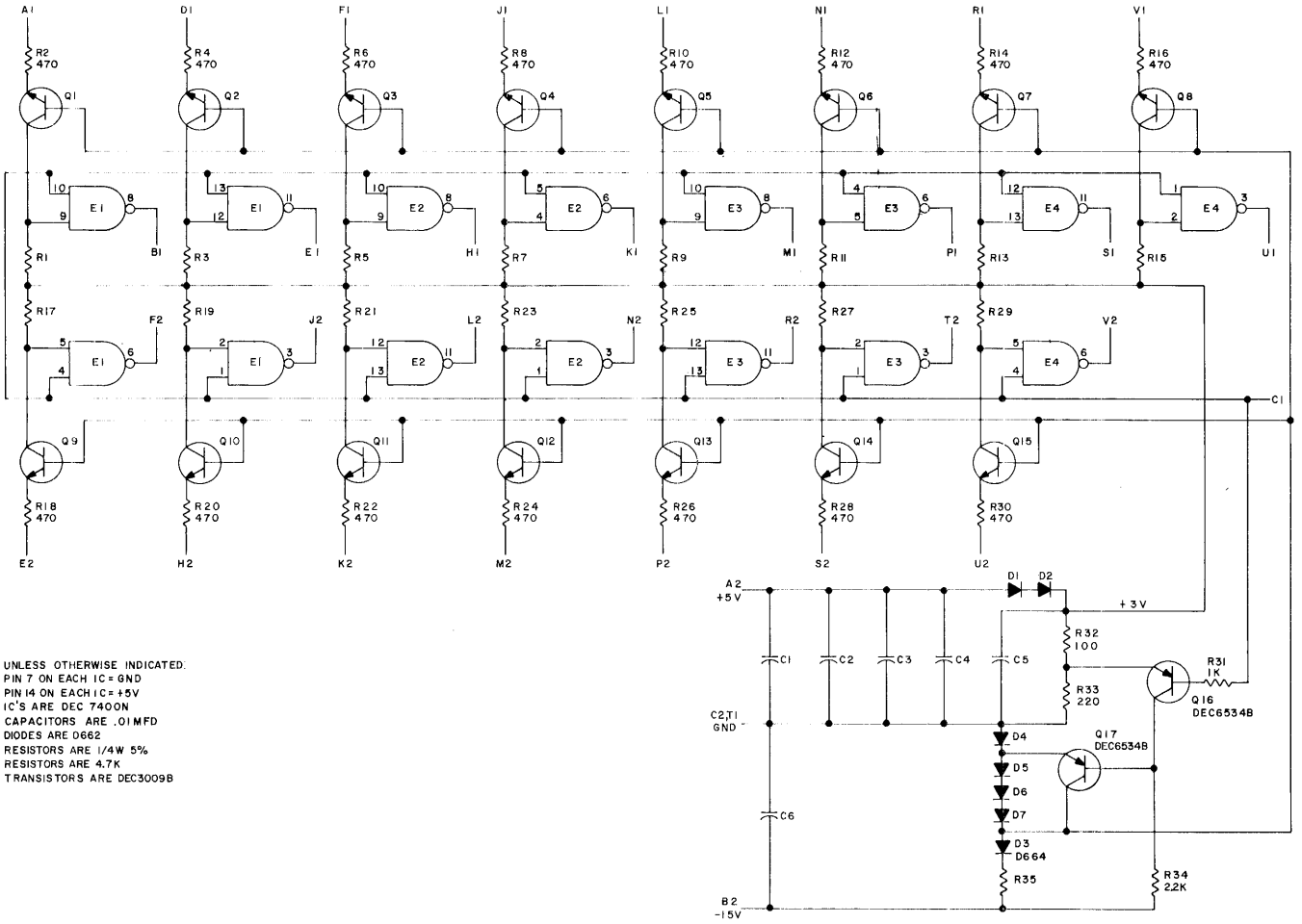

UNLESS OTHERWISE INDICATED:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
IC'S ARE DEC 7400N
CAPACITORS ARE .01 MFD
DIODES ARE D662
RESISTORS ARE 1/4W 5%
RESISTORS ARE 4.7K
TRANSISTORS ARE DEC3009B

REVISIONS		
CHK	CHG NO.	REV.

DRN. [signature] DATE 3-27-69
CHK'D M. Marchand DATE 3/28/69
ENG. R. Vajdsang DATE 7/11/69
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	1N645		
D664	1N3606		
DEC3009B	2N3009		
DEC6534B	MPS6534		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE BUS DATA INTERFACE M100

SIZE	CODE	NUMBER	REV.
C	CS	M100-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRC 102

DIST 324, 439, 435 PINK 5/

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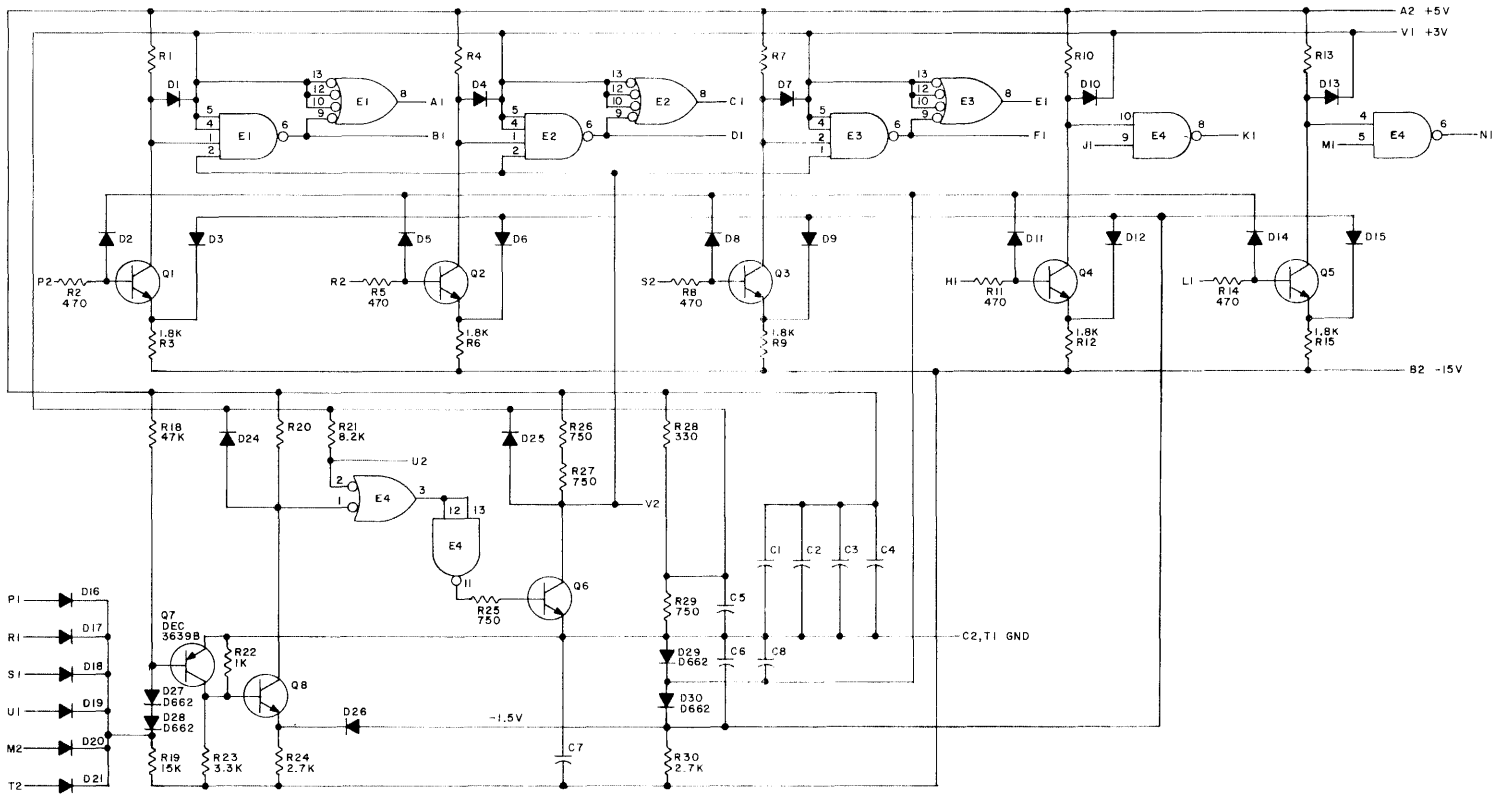

UNLESS OTHERWISE INDICATED:
DIODES ARE D664
RESISTORS ARE 1.5K; 1/4W, 5%
CAPACITORS ARE .01 MFD 100V 20%
TRANSISTORS ARE DEC3009B
E1, E2, E3 ARE DEC74H40N
E4 IS DEC7400N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REVISIONS		
CHK	CHG NO.	REV.

DRN	M. Dallen	DATE 4-2-69
CHKD	[illegible]	DATE 4-4-69
ENG	R. Vogelsang	DATE 5/6/69
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	1N645		
D664	1N3606		
DEC3009B	2N3009		
DEC3639B	2N3639		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: DEVICE SELECTOR M102

SIZE	CODE	NUMBER	REV.
C	CS	M102-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRC 102

5 DIST. 324, 434, 435 PINK

SIZE C CODE CS NUMBER M102-0-1 REV.

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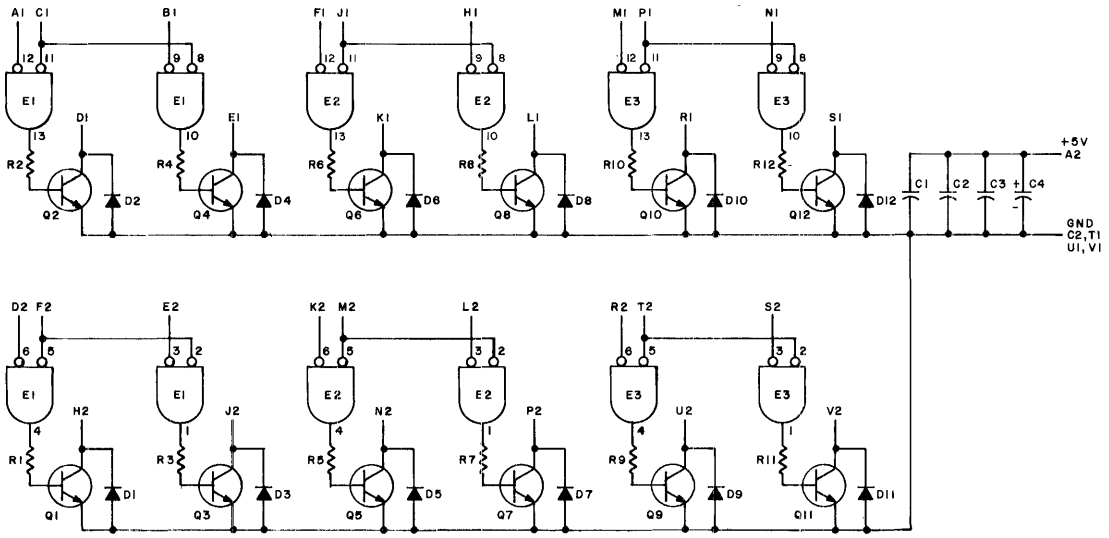

NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
E1 - E3	INTEGRATED CKT. DEC7402N	1909004
Q1 - Q12	TRANSISTOR DEC3009B	1503100
R1 - R12	RES. 390 1/4W 5% CC	1300309
D1 - D12	DIODE D664	1100114
C4	CAP. 6.8MFD 35V 20% S.TANT	1000067
C1 - C3	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M623-0-0

PARTS LIST

REVISIONS			
CHK	CHG NO	REV	
	00002	B	
	00003	D	

DRN. M. Haller DATE 6-4-68
CHK'D DATE 6/10/68
ENG. DATE 7/1/68
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	1N3606		
DEC3009B	2N3009		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE BUS DRIVER M623

SIZE C | CODE CS | NUMBER M623-0-1 | REV. D

PRINTED CIRCUIT REV. D

DEC FORM NO. DRC 102

PINK 5

DIST. 324 434 433

SIZE C | CODE CS | NUMBER M623-0-1 | REV. D

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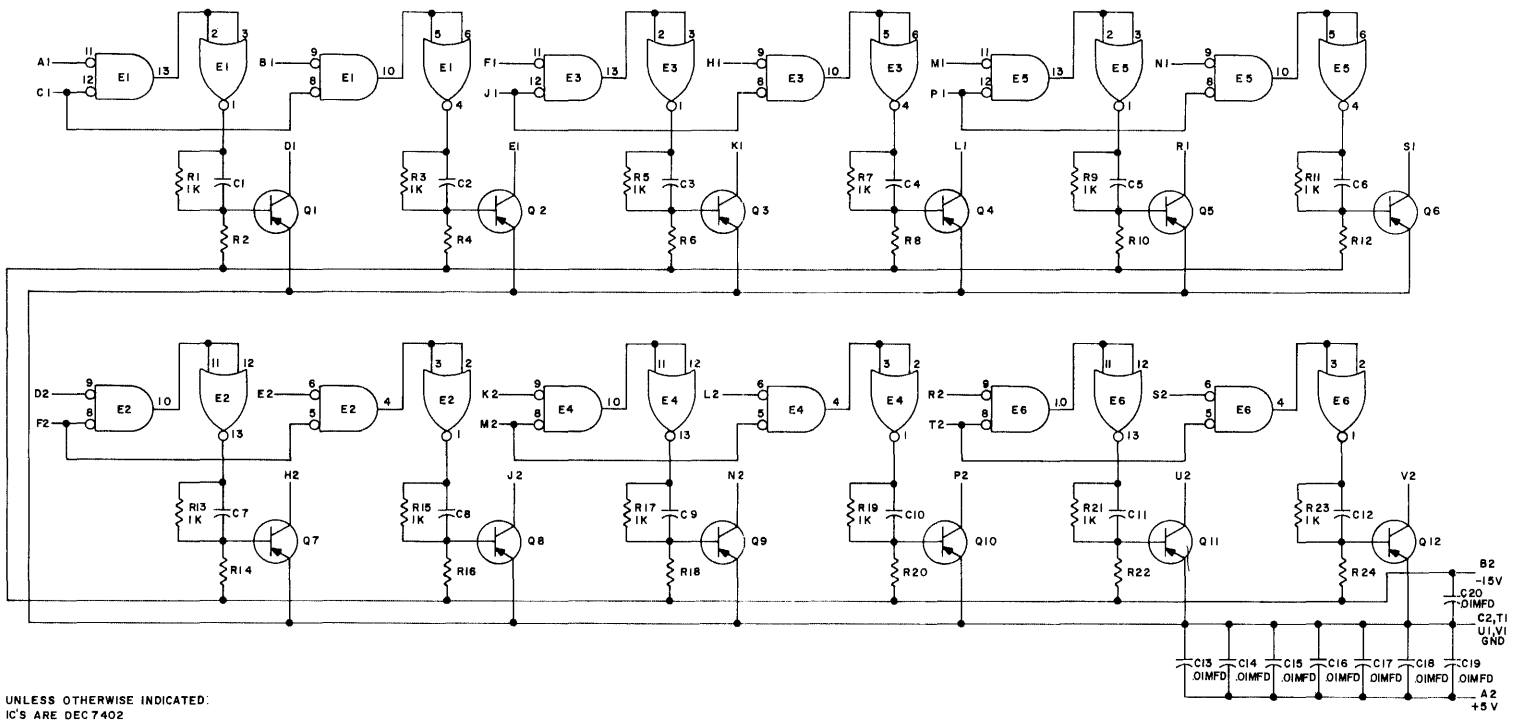


UNLESS OTHERWISE INDICATED:
IC'S ARE DEC 7402
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
CAPACITORS ARE 15 MMF
RESISTORS ARE 5.6K, 1/4W, 5%
TRANSISTORS ARE DEC 3639B

REVISIONS | CHK | CHG NO. | REV.

DRN		DATE 3-5-69
CHK'D		DATE 3-6-69
ENG.		DATE 7/11/69
PROD.		DATE 8/5/69

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DE3639B	2N3639		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: NEGATIVE BUS DRIVER M633

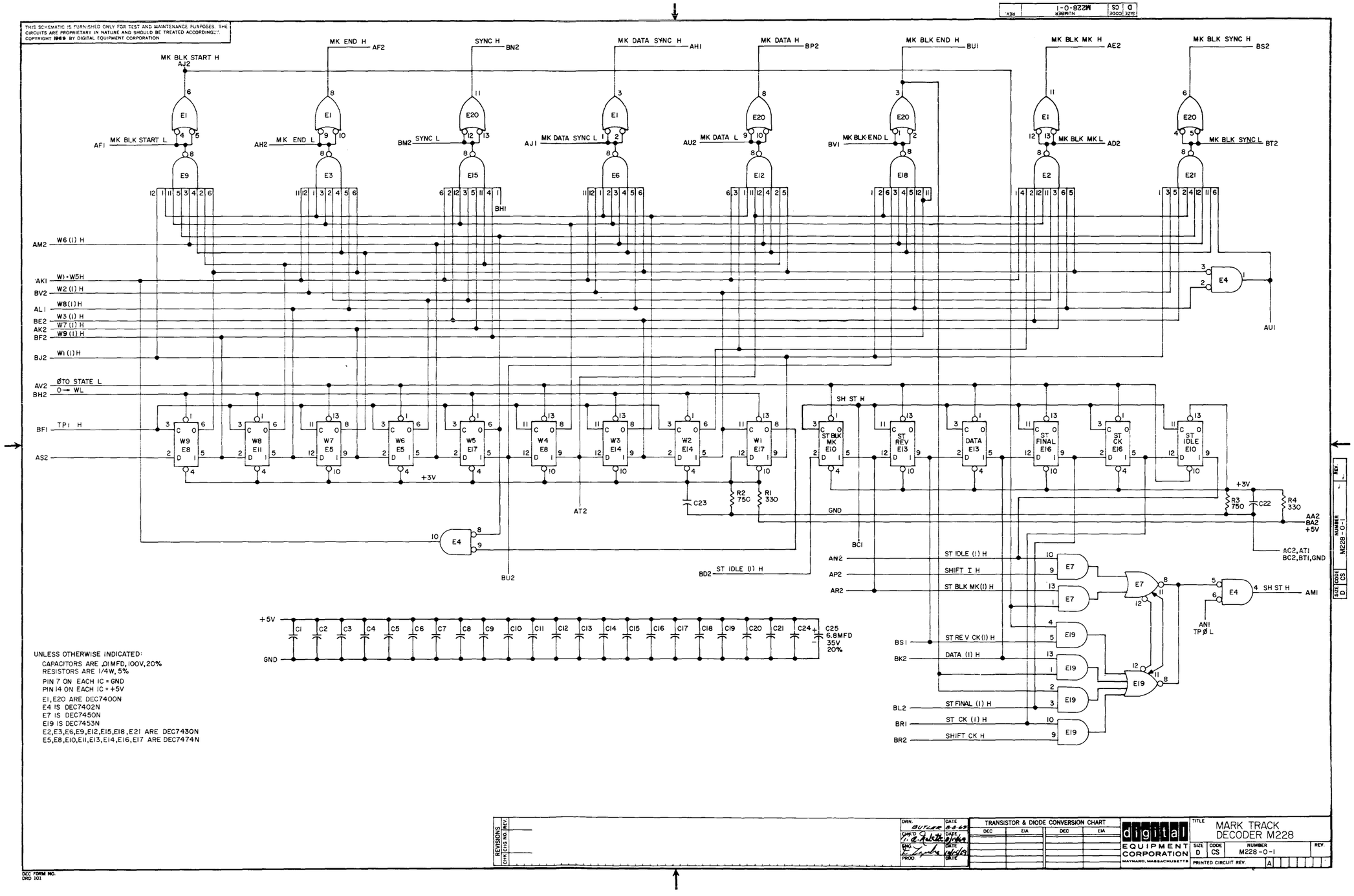
SIZE	CODE	NUMBER	REV.
C	CS	M633-0-1	

PRINTED CIRCUIT REV. A B

SIZE C | CODE C.I. CS | NUMBER M633-0-1 | REV.

DEC FORM NO. DRC 102

E. PINK DIST: 324, 631, 435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MK BLK START H
MK END H
SYNC H
MK DATA SYNC H
MK DATA H
MK BLK END H
MK BLK MK H
MK BLK SYNC H
MK BLK START L
MK END L
SYNC L
MK DATA SYNC L
MK DATA L
MK BLK END L
MK BLK MK L
MK BLK SYNC L
W6 (1) H
W1 • W5H
W2 (1) H
W8 (1) H
W3 (1) H
W7 (1) H
W9 (1) H
W1 (1) H
ØTO STATE L
0 → WL
TP1 H
SH ST H
ST IDLE (1) H
SHIFT I H
ST BLK MK (1) H
ST REV CK (1) H
DATA (1) H
ST FINAL (1) H
ST CK (1) H
SHIFT CK H
AC2, AT1
BC2, BT1, GND
AA2
BA2
+5V
GND
C25
6.8MFD
35V
20%
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD, 100V, 20%
RESISTORS ARE 1/4W, 5%
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E20 ARE DEC7400N
E4 IS DEC7402N
E7 IS DEC7450N
E19 IS DEC7453N
E2, E3, E6, E9, E12, E15, E18, E21 ARE DEC7430N
E5, E8, E10, E11, E13, E14, E16, E17 ARE DEC7474N
TRANSISTOR & DIODE CONVERSION CHART
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
MARK TRACK
DECODER M228
SIZE D
CODE CS
NUMBER M228-0-1
PRINTED CIRCUIT REV. A
DEC FORM NO. DRD 101

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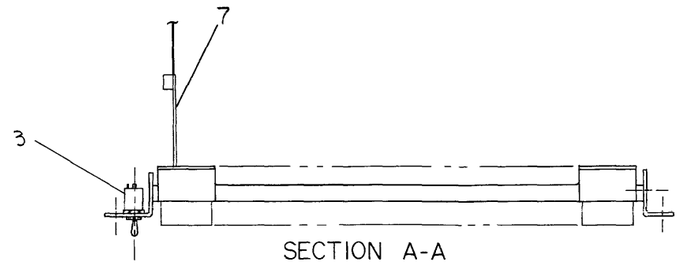
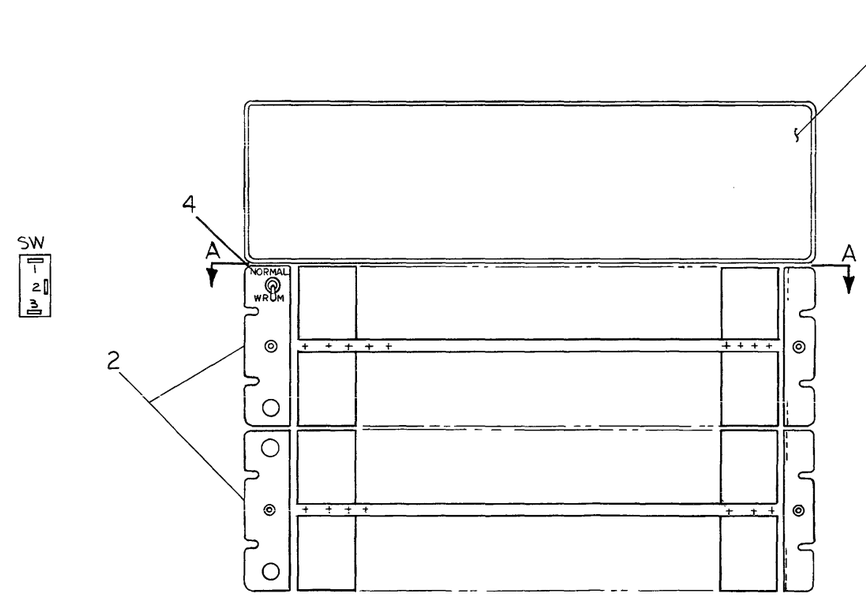
LEGEND	
NUMBER	VARIATION
TCØ8-Ø	60 H.Z
TCØ8-A	50 H.Z

WIRE TABLE

ITEM NO	DESCRIPTION AWG	COLOR	CONNECTIONS FROM	TO	REMARKS
5	24	BLACK	SW-2	BØ1C2	
6	24	YEL	SW-3	BØ8V1	



SECTION A-A



QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

FIRST USED ON OPTION/MODEL: TCØ8

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

DRN. DATE 6/19/69
CHK'D. DATE 6/8/69
ENG. DATE
PROJ. ENG. DATE
PROD. DATE 9/2/69

NEXT HIGHER ASSY: A-ML-TCØ8-Ø-Ø
SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: DECTAPE CONTROL

SIZE D | CODE UA | NUMBER TCØ8-Ø-Ø | REV A
DIST. G

REVISIONS

CHK	CHANGE NO.	REV.
	TCØ8-00003	A

D. LAZUKA 1-17-70

DEC FORM NO. DRD 100

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NOTE:
TC08N ONLY

I/O BMB 03 (1)L P1
I/O BMB 04 (1)L R1
I/O BMB 05 (1)L S1
I/O BMB 06 (1)L U1
I/O BMB 07 (1)L M2
I/O BMB 08 (0)L T2
M102 C04

IOP 1 H P2 — M103 C04 — B1 RSTA L, A1 RSTA H
IOP 2 H R2 — M103 C04 — D1 CSTA L, C1 CSTA H
IOP 4 H S2 — M103 C04 — F1 XSTA L, E1 XSTA H

I/O BMB 03 (1)H D2
I/O BMB 04 (1)H E2
I/O BMB 05 (1)H F2
I/O BMB 06 (1)H H2
I/O BMB 07 (1)H J2
I/O BMB 08 (0)H K2
+3V C08U1 H L2
+3V C08U1 H N2
M103 C04 — V2 76 H, U2 +3V C08U1 H

+3V D10U1 H D1, F2, K1
BAC 06 (1)H C1 — MF00 M206 D11 — E1
BAC 07 (1)H E2 — MF01 M206 D11 — H2
BAC 08 (1)H J1 — MF02 M206 D11 — L1
LDMF H B1
A1 PWR CLR L
+3V D10U1 H K2 — WC M206 D11 — U1
XSTA H N1
WCO L R1
M121 C08 — U1 +3V C08U1 H

XSTA L H2, J2, K2 — M602 D13 — F2; E2 D2
M627 D12 — A1, B1, C1, D1 — E1 B-XSTA H

-XSTA L P2, N2, M2 — M602 D13 — L2 XSAD L; R2 S2
M111 A11 — K2 — L2 XSAD H

I/O TS03 H H1
+3V C08U1 H J1
M103 C04 — K1 TS03 L

I/O BWCO L F1
+3V C08U1 H C1
M101 C01 — H1 WCO H M2
M111 C06 — N2 WCO L

I/O B-BRK (0)L D1
+3V C08U1 H C1
M101 C01 — E1 B-BRK H
M627 B10 — R2, S2, T2, U2 — V2 B-BRK (1)L

76 H S2
M111 C06 — T2
76 L R2
77 L S2
M627 D12 — T2, U2 — V2 76 + 77 H
77 H U2
M111 C06 — V2

SH ST H A1
M111 C17 — B1
M627 C16 — K2, L2, M2, N2 — P2 SH ST-B H

B-BRK H M1
T3 H N1
P1
FR 01 (1)H R1
M627 D12 — S1 BMB TO DTB L
M627 D12 — F1, H1, J1, K1 — L1 BMB TO DTB H

-ADDR ACC L N1
M111 C17 — P1 -ADDR ACC H

NOTE:
TC08N ONLY

I/O BMB 03 (1)L P1
I/O BMB 04 (1)L R1
I/O BMB 05 (1)L S1
I/O BMB 06 (1)L U1
I/O BMB 07 (1)L M2
I/O BMB 08 (1)L T2
M102 C05

IOP 1 H P2 — M103 C05 — B1 DTSF L, A1 DTSF H
IOP 2 H R2 — M103 C05 — D1 RSTB L, C1 RSTB H
IOP 4 H S2 — M103 C05 — F1 LDMF L, E1 LDMF H

I/O BMB 03 (1)H D2
I/O BMB 04 (1)H E2
I/O BMB 05 (1)H F2
I/O BMB 06 (1)H H2
I/O BMB 07 (1)H J2
I/O BMB 08 (1)H K2
+3V C08U1 H L2
+3V C08U1 H N2
M103 C05 — V2 77 H, U2 +3V C08U1 H

TS03 L H2, J2, K2 — M602 D17 — F2; E2 D2
M111 C17 — R1 — S1 T3 H

I/O B-RUN (0)L A1
+3V C08U1 H C1
M101 C01 — B1 B-RUN (1)H

I/O PWR CLR H H1
+3V C08U1 H J1
M103 C05 — K1 PWR CLR L

PWR CLR L P2
M111 C05 — R2 PWR CLR H

EF (1)L L1
DTF (1)L M1
M113 A12 — N1
ENI (1)H H1
M113 A12 — J1 — K1 INT RQ L
P1
DTSF H R1
M113 A12 — S1 SKP RQ L

LDMF L P2
XSTA L R2
M113 B08 — S2; S2 — T2 Ø TO AC L
M111 B06

REVISIONS		
CHK	CHANGE NO.	REV.
NR	TC08-00001	A
	R SOFKA 10/2/69	
	D LAZUKA 10/6/69	
NR	TC08-00002	B
	K COTE 12-9-69	
	D LAZUKA	
	TC08-00004	C

DRN D.SHEPARD	DATE 6/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHKD N.RHEAULT	DATE 6/24/69	
ENG D.LAZUKA	DATE 6/24/69	TITLE I/O CONTROL
PROJ ENG D.LHZUKA	DATE 9/2/69	
PROD P.LASKEY	DATE 9/2/69	
FIRST USED ON TC08		SIZE D; CODE BS; NUMBER TC08-0-1; REV. C
SCALE		
SHEET 1 OF 1		DIST.

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+3V A09U1 H — M161 A07 — R1 R2 P1 P2 L1 07 L, L2 07 H, H1 06 L, H2 06 H, M1 05 L, M2 05 H, F1 04 L, F2 04 H, N1 03 L, N2 03 H, J1 02 L, J2 02 H, E1 01 L, E2 01 H, D1 00 L, D2 00 H

USR 00 (1)H — U1 V2 — 2²
USR 01 (1)H — U2 — 2¹
USR 02 (1)H — V1 — 2⁰

M117 A09 U1 +3V A09U1 H

M121 D09 U1 +3V D09U1 H

T WRITE OK L — W005 B23 L2 H2 — M502 A22 D2 WRITE OK H — E2

BAC 00 (1)H — USR 00 M207 B07 — D1 E1 B1 C1 K 0 F1 A1
BAC 01 (1)H — USR 01 M207 B07 — F2 H2 D2 E2 K 0 J2
BAC 02 (1)H — USR 02 M207 B07 — K1 L1 H1 J1 K 0 M1
BAC 03 (1)H — MR00 M207 B07 — N2 P2 L2 M2 K 0 R2 — K2 0 TO STA L

+3V B12 U1H — N2
BAC 04 (1)H — MR01 M207 C07 — N2 P2 L2 M2 K 0 R2 — K2 M-STOP L
BMR00 M205 B14 — D 1 P2 M2 C 0 R2 — K2
BMR01 M205 B14 — +3V B12 U1H A1 D 1 F1 C1 B1 C 0 E1 — D1
X SA DY H L2

XSTA H

BAC 05 (1)H — FR 00 M207 B07 — R1 S1 N1 P1 K 0 U1 — K2
BAC 06 (1)H — FR 01 M207 B07 — U2 V2 S2 T2 K 0 V1 — K2
BAC 07 (1)H — FR 02 M207 C07 — D1 E1 B1 C1 K 0 F1 — A1
BAC 08 (1)H — FR 03 M207 C07 — F2 H2 D2 E2 K 0 J2
BAC 09 (1)H — ENI M207 C07 — K1 L1 H1 J1 K 0 M1 — 0 TO STA L

WRTM L H2 — M113 B08 — K2 WRTM + FR03 H
FR 03 (1)L J2
READ DATA L L2 — M113 B08 — N2 RD + WD H
WRITE DATA L M2

BMR 01 (1)L A1 — M633 A23 — W005 B23 D1 D2 — T GO L
BMR 01 (0)L B1 — M633 A23 — W005 B23 E1 E2 — T STOP L
BMR00 (0)L F1 — M633 A23 — W005 B23 K1 H2 — T FWD L
BMR00 (1)L H1 — M633 A23 — W005 B23 L1 J2 — T REV L
PWR CLR L M1 — M633 A23 — W005 B23 R1 K2 — T PWR CLR L
Ø1 L N1 — M633 A23 — W005 B23 S1 M2 — T Ø1 L
Ø2 L D2 — M633 A23 — W005 B23 H2 N2 — T Ø2 L
Ø3 L E2 — M633 A23 — W005 B23 J2 P2 — T Ø3 L
Ø4 L K2 — M633 A23 — W005 B23 N2 R2 — T Ø4 L
M2 — M633 A23 — W005 B23 P2 S2 — T Ø5 L
Ø5 L L2
Ø6 L R2 — M633 A23 — W005 B23 U2 T2 — T Ø6 L
T2
Ø7 L S2 — M633 A23 — W005 B23 V2 U2 — T Ø7 L
R2 — M633 B22 — U2
T2 — W005 B23
Ø0 L S2 — M633 B22 — V2 V2 — T Ø0 L

+3V D09U1 H — M161 D07 — R1 R2 P1 P2 L1 SE L, L2 SE H, H1 WRTM L, H2 WRTM H, M1 WRITE ALL L, M2 WRITE ALL H, F1 WRITE DATA L, F2 WRITE DATA H, N1 READ ALL L, N2 READ ALL H, J1 READ DATA L, J2 READ DATA H, E1 SEARCH L, E2 SEARCH H, D1 MOVE L, D2 MOVE H

FR 01 (1)H — U1 V2 — 2²
FR 02 (1)H — U2 — 2¹
FR 03 (1)H — V1 — 2⁰

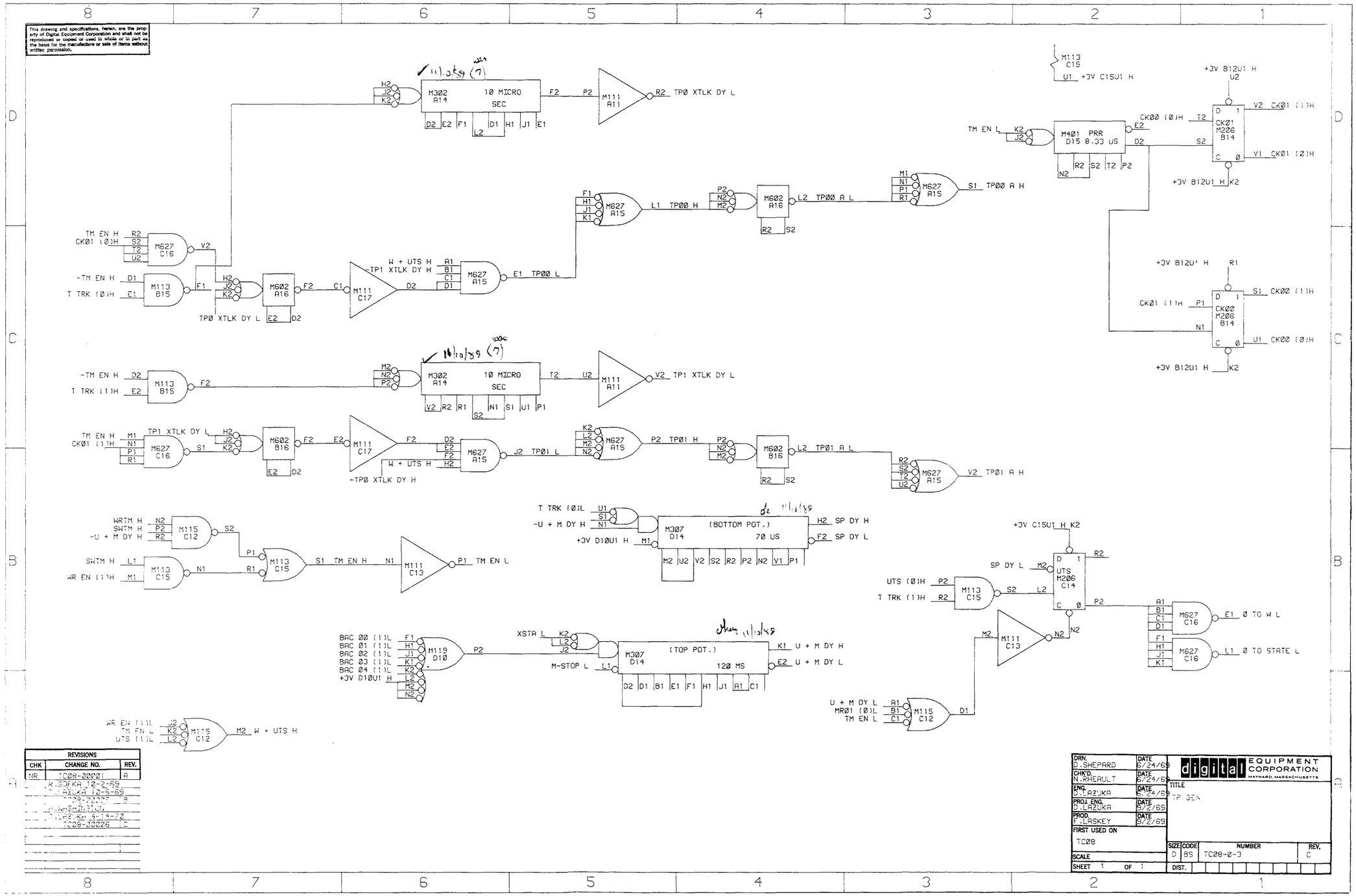
Ø TO STA H

CSTA L L2
PWR CLR L M2 — M113 A10 — N2 — N1 — M111 A11 — P1 Ø TO STA L

B-RUN (1)H N2
Ø TO STA L P2
PC + ES L R2 — M115 B11 — S2 — R1 — M111 A11 — S1 M-STOP L

REVISIONS		
CHK	CHANGE NO.	REV.
NR	TC08-00001	A
	R SOFKA 10/2/69	
	D LAZUKA 10/5/69	
NR	TC08-00002	B
	K COTE	
	D LAZUKA	
	TC08-00004	C
	K COTE 1-28-70	

DRN. D.SHEPARD	DATE 6/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHKD. N.MHEAULT	DATE 6/24/69	
ENG. D.LAZUKA	DATE 6/24/69	TITLE STATUS 'A'
PROJ. ENG. D.LAZUKA	DATE 9/2/69	
PROD. F.CASKEY	DATE 9/2/69	
FIRST USED ON TC08		SIZE D · CODE 85 · NUMBER TC08-0-2 · REV. C
SCALE		
SHEET 1 OF 1		DIST.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M302 A14 10 MICRO SEC
M111 A11
R2 TP0 XTLK DY L
M113 C15
U1 +3V C15U1 H
+3V B12U1 H
U2
CK01 M206 B14
V2 CK01 (1)H
V1 CK01 (0)H
CK00 (0)H
TM EN L
M401 PRR D15 8.33 US
M627 A15
S1 TP00 A H
L1 TP00 H
M602 A16
L2 TP00 A L
M627 C16
TM EN H
CK01 (0)H
-TM EN H
T TRK (0)H
M113 B15
TP0 XTLK DY L
M111 C17
W + UTS H
-TP1 XTLK DY H
E1 TP00 L
CK00 M206 B14
S1 CK00 (1)H
U1 CK00 (0)H
CK01 (1)H
T TRK (1)H
TP1 XTLK DY L
M602 B16
J2 TP01 L
-TP0 XTLK DY H
P2 TP01 H
L2 TP01 A L
V2 TP01 A H
WRTM H
SWTM H
-U + M DY H
M115 C12
SWTM H
WR EN (1)H
M113 C15
TM EN H
M111 C13
P1 TM EN L
T TRK (0)L
-U + M DY H
+3V D10U1 H
M307 D14 (BOTTOM POT.) 70 US
H2 SP DY H
F2 SP DY L
+3V C15U1 H K2
UTS (0)H
T TRK (1)H
UTS M206 C14
SP DY L
M627 C16
E1 0 TO W L
L1 0 TO STATE L
BAC 00 (1)L
BAC 01 (1)L
BAC 02 (1)L
BAC 03 (1)L
BAC 04 (1)L
+3V D10U1 H
M119 D10
XSTA L
M-STOP L
M307 D14 (TOP POT.) 120 MS
K1 U + M DY H
E2 U + M DY L
U + M DY L
MR01 (0)L
TM EN L
WR EN (1)L
TM EN L
UTS (1)L
M2 W + UTS H
REVISIONS
CHK
CHANGE NO.
REV.
NR
TC08-00001
A
R.SOFKA 10-2-69
D.LAZUKA 10-6-69
TC08-00006
C
DRN. D.SHEPARD
DATE 6/24/69
CHK'D. N.RHEAULT
DATE 6/24/69
ENG. D.LAZUKA
DATE 6/24/69
PROJ. ENG. D.LAZUKA
DATE 9/2/69
PROD. F.LASKEY
DATE 9/2/69
FIRST USED ON TC08
SCALE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE TP GEN
SIZE D
CODE BS
NUMBER TC08-0-3
REV. C
DIST.

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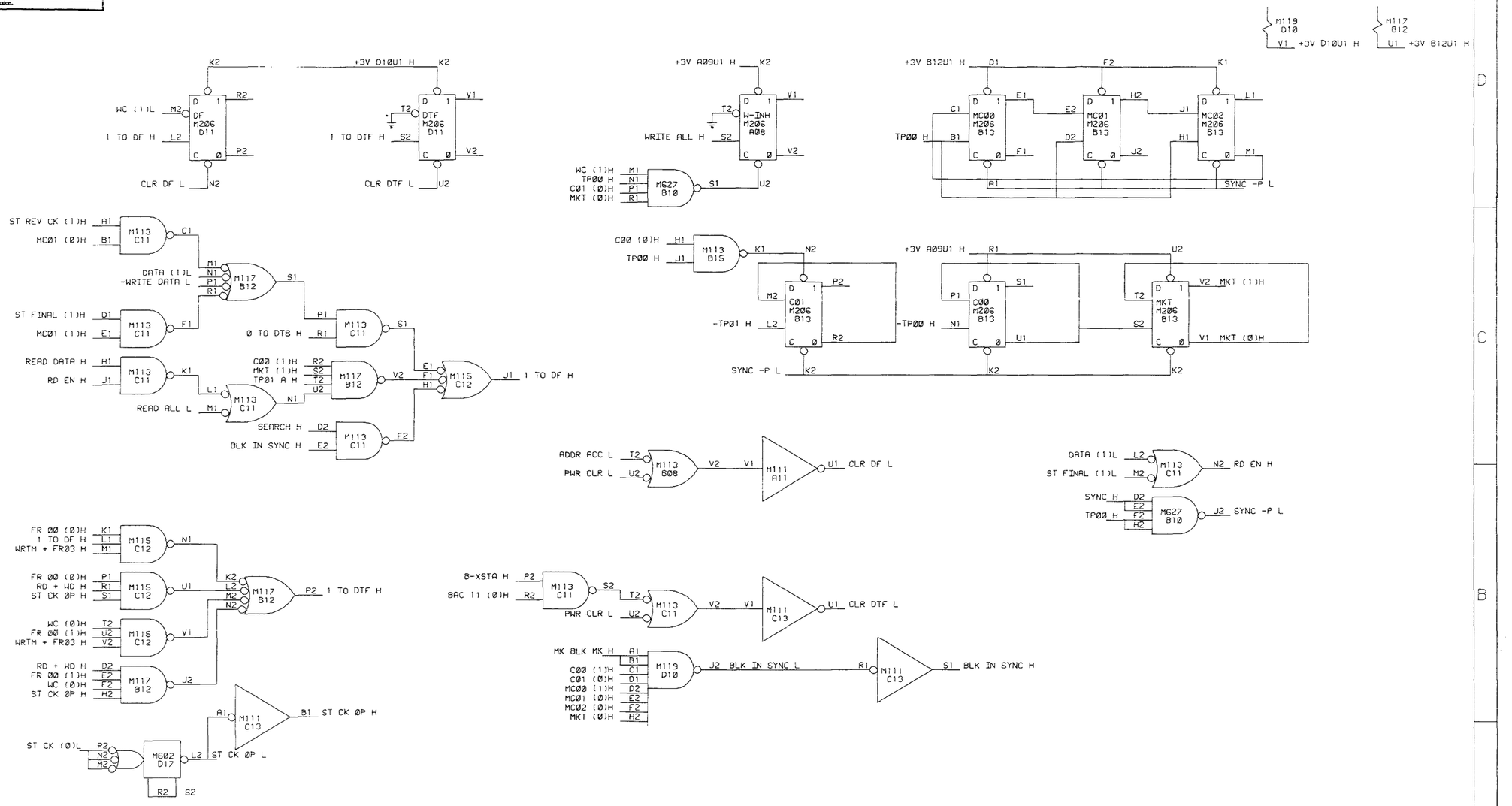
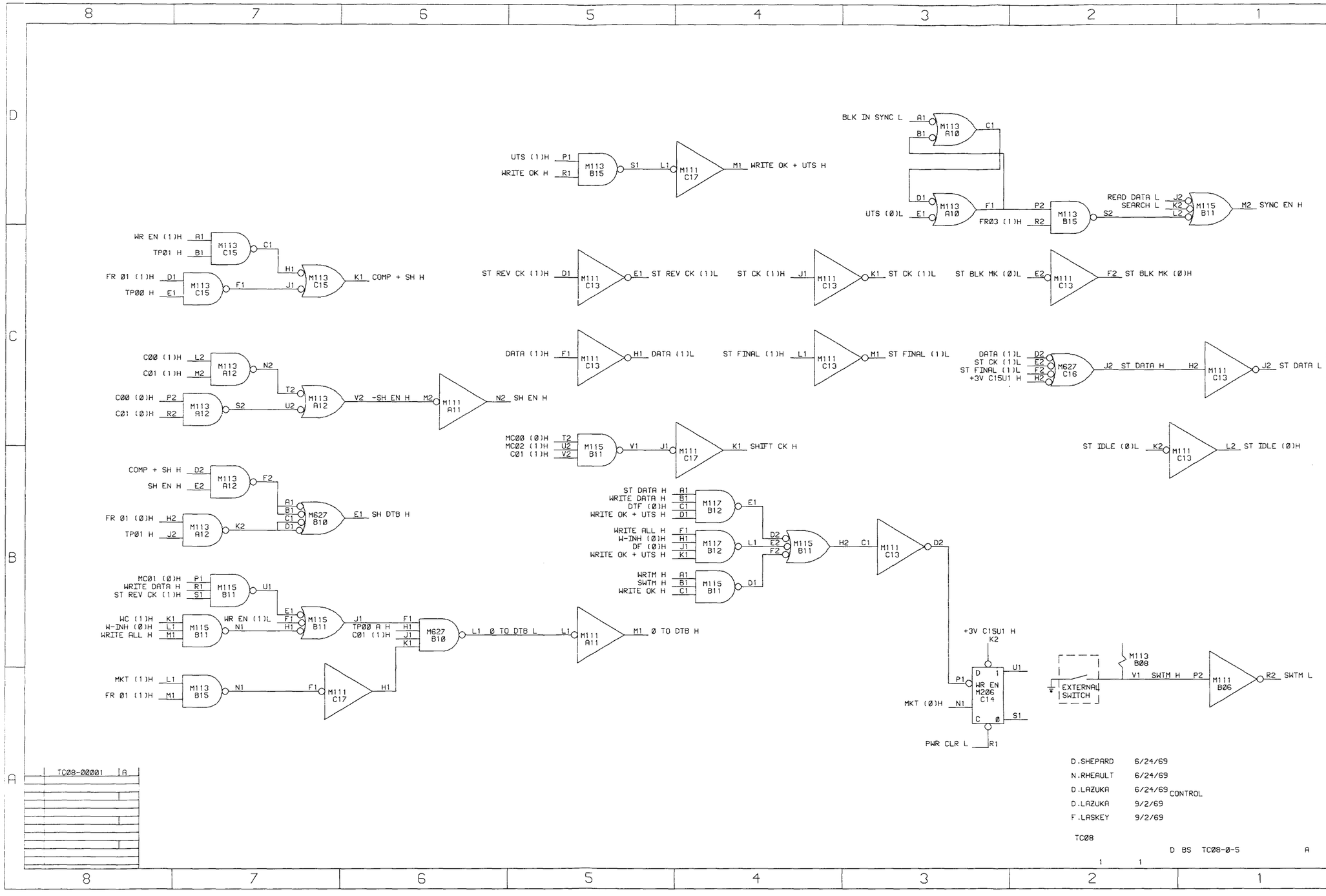


REVISIONS		
CHK	CHANGE NO.	REV.
NR	TC08-00001	A
	R.SOUKA 10-2-69	
	D.LAZUKA 10-6-69	
	TC08-00005	B

DRN. D.SHEPARD	DATE 6/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. N.RHEAULT	DATE 6/24/69	
ENG. D.LAZUKA	DATE 6/24/69	TITLE FLAGS
PROJ. ENG. D.LAZUKA	DATE 9/2/69	
PROD. T.ASKEY	DATE 9/2/69	
FIRST USED ON TC08		SIZE D CODE BS NUMBER TC08-0-4 REV. B
SCALE		
SHEET 1 OF 1		DIST.


BLK IN SYNC L
M113 A10
UTS (1)H
WRITE OK H
M113 B15
M111 C17
M1 WRITE OK + UTS H
UTS (Ø)L
FRØ3 (1)H
READ DATA L
SEARCH L
M115 B11
M2 SYNC EN H
WR EN (1)H
TPØ1 H
M113 C15
FR Ø1 (1)H
TPØØ H
K1 COMP + SH H
ST REV CK (1)H
M111 C13
ST REV CK (1)L
ST CK (1)H
ST CK (1)L
ST BLK MK (Ø)L
F2 ST BLK MK (Ø)H
DATA (1)H
H1 DATA (1)L
ST FINAL (1)H
M1 ST FINAL (1)L
DATA (1)L
ST CK (1)L
ST FINAL (1)L
+3V C15U1 H
M627 C16
J2 ST DATA H
J2 ST DATA L
CØØ (1)H
CØ1 (1)H
M113 A12
CØØ (Ø)H
CØ1 (Ø)H
M111 A11
N2 SH EN H
MCØØ (Ø)H
MCØ2 (1)H
CØ1 (1)H
M115 B11
SHIFT CK H
ST IDLE (Ø)L
L2 ST IDLE (Ø)H
COMP + SH H
SH EN H
FR Ø1 (Ø)H
TP01 H
M627 B10
E1 SH DTB H
ST DATA H
WRITE DATA H
DTF (Ø)H
WRITE OK + UTS H
M117 B12
WRITE ALL H
W-INH (Ø)H
DF (Ø)H
WRITE OK + UTS H
WRTM H
SWTM H
WRITE OK H
M115 B11
M111 C13
MCØ1 (Ø)H
WRITE DATA H
ST REV CK (1)H
WC (1)H
W-INH (Ø)H
WRITE ALL H
WR EN (1)L
TPØØ A H
CØ1 (1)H
L1 Ø TO DTB L
M1 Ø TO DTB H
MKT (1)H
FR Ø1 (1)H
+3V C15U1 H
WR EN M206 C14
MKT (Ø)H
PWR CLR L
EXTERNAL SWITCH
M113 BØ8
V1 SWTM H
M111 BØ6
R2 SWTM L
TC08-00001 A
D.SHEPARD 6/24/69
N.RHEAULT 6/24/69
D.LAZUKA 6/24/69 CONTROL
D.LAZUKA 9/2/69
F.LASKEY 9/2/69
TC08
D 8S TC08-0-5 A

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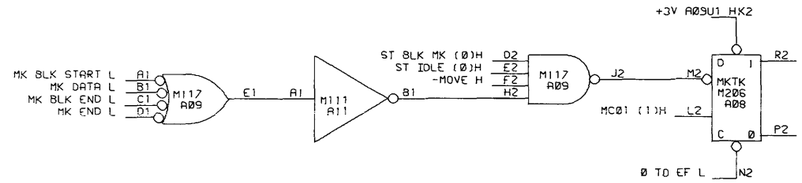
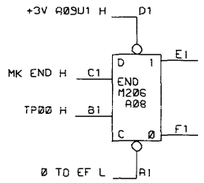
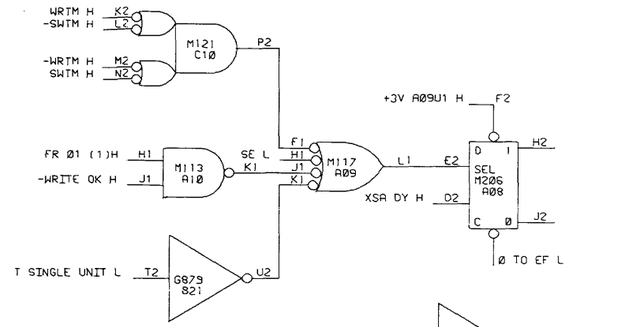
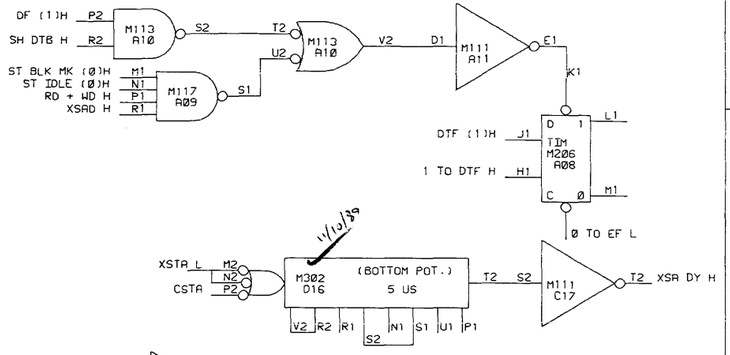
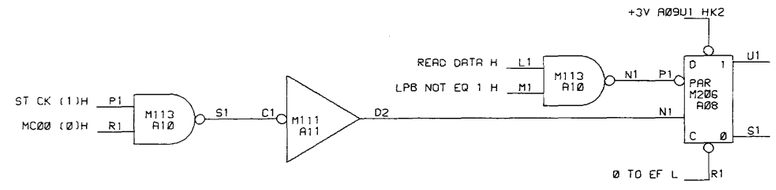
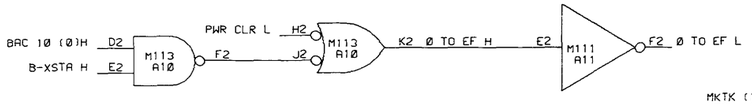


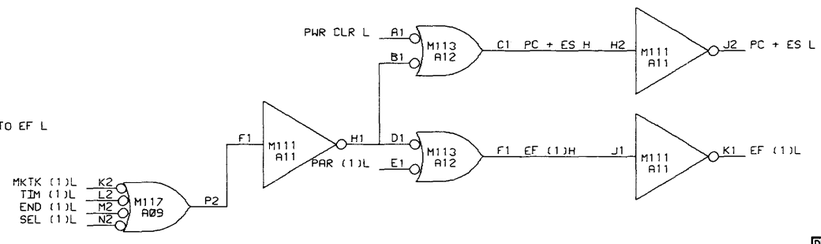






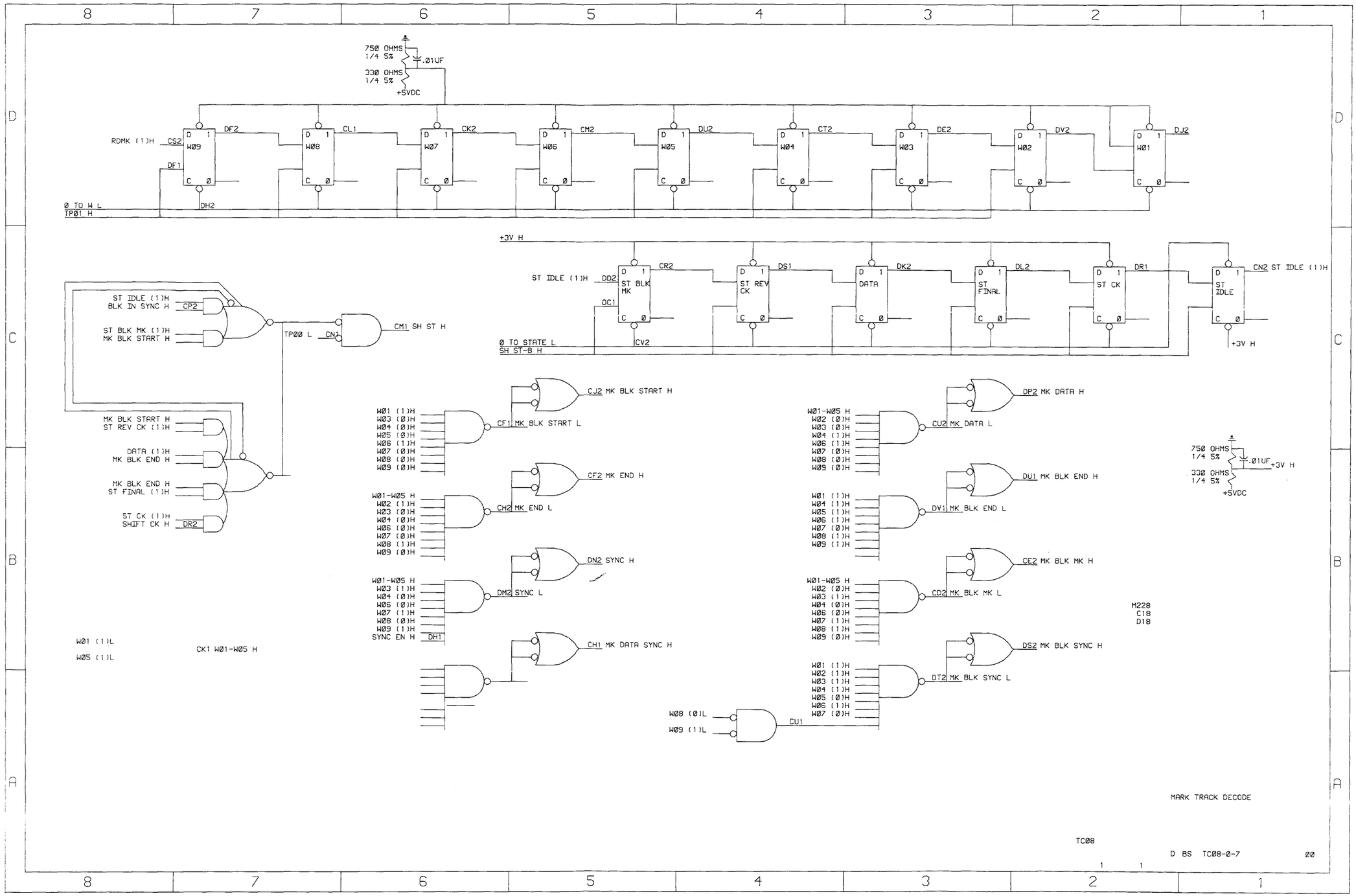


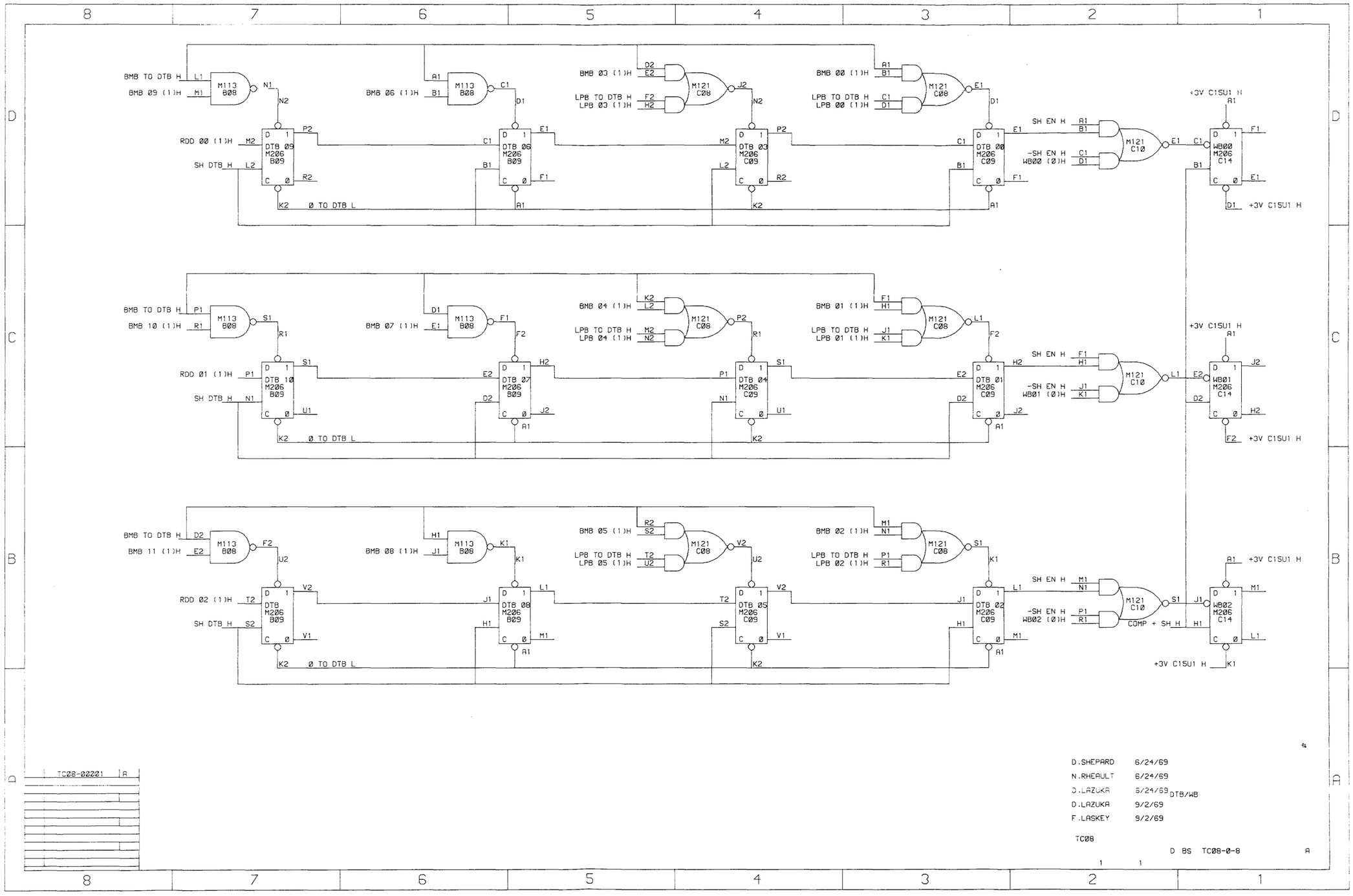




REVISIONS		
CHK	CHANGE NO.	REV.
NR	TC08-00001	A
	R.SOFKA 10-2-69	
	D.LAZUKA 10-6-69	
	TC08-00005	B

DRN. D.SHEPARD	DATE 5/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. N.RHEAULT	DATE 5/24/69	
ENG. D.LAZUKA	DATE 5/24/69	TITLE ERRORS
PROJ. ENG. D.LAZUKA	DATE 5/27/69	
PROD. F.LASKEY	DATE 5/27/69	
FIRST USED ON TC08		SIZE D CODE BS NUMBER TC08-Ø-6 REV. B
SCALE		
SHEET 1 OF 1		DIST.


750 OHMS 1/4 5%
.01UF
330 OHMS 1/4 5%
+5VDC
RDMK (1)H
CS2
DF1
DF2
CL1
CK2
CM2
DU2
CT2
DE2
DV2
DJ2
W09
W08
W07
W06
W05
W04
W03
W02
W01
D 1
C 0
Ø TO W L
TP01 H
DH2
+3V H
ST IDLE (1)H
DD2
DC1
CR2
DS1
DK2
DL2
DR1
CN2 ST IDLE (1)H
ST BLK MK
ST REV CK
DATA
ST FINAL
ST CK
ST IDLE
Ø TO STATE L
SH ST-B H
CV2
ST IDLE (1)H
BLK IN SYNC H
CP2
ST BLK MK (1)H
MK BLK START H
TP00 L
CN1
CM1 SH ST H
MK BLK START H
ST REV CK (1)H
DATA (1)H
MK BLK END H
MK BLK END H
ST FINAL (1)H
ST CK (1)H
SHIFT CK H
DR2
W01 (1)L
W05 (1)L
CK1 W01-W05 H
W01 (1)H
W03 (Ø)H
W04 (Ø)H
W05 (Ø)H
W06 (1)H
W07 (Ø)H
W08 (Ø)H
W09 (Ø)H
CF1 MK BLK START L
CJ2 MK BLK START H
W01-W05 H
W02 (1)H
W03 (Ø)H
W04 (Ø)H
W06 (Ø)H
W07 (Ø)H
W08 (1)H
W09 (Ø)H
CH2 MK END L
CF2 MK END H
W01-W05 H
W03 (1)H
W04 (Ø)H
W06 (Ø)H
W07 (1)H
W08 (Ø)H
W09 (1)H
SYNC EN H
DM2 SYNC L
DN2 SYNC H
DH1
CH1 MK DATA SYNC H
W01-W05 H
W02 (Ø)H
W03 (Ø)H
W04 (1)H
W06 (1)H
W07 (Ø)H
W08 (1)H
W09 (Ø)H
CU2 MK DATA L
DP2 MK DATA H
W01 (1)H
W04 (1)H
W05 (1)H
W06 (1)H
W07 (Ø)H
W08 (1)H
W09 (1)H
DV1 MK BLK END L
DU1 MK BLK END H
W01-W05 H
W02 (Ø)H
W03 (1)H
W04 (Ø)H
W06 (Ø)H
W07 (1)H
W08 (1)H
W09 (Ø)H
CD2 MK BLK MK L
CE2 MK BLK MK H
W01 (1)H
W02 (1)H
W03 (1)H
W04 (1)H
W05 (Ø)H
W06 (1)H
W07 (Ø)H
DT2 MK BLK SYNC L
DS2 MK BLK SYNC H
W08 (Ø)L
W09 (1)L
CU1
750 OHMS 1/4 5%
.01UF
+3V H
330 OHMS 1/4 5%
+5VDC
M22Ø
C18
D18
MARK TRACK DECODE
TC08
D BS TC08-0-7
ØØ



BMB TO DTB H
BMB 09 (1)H
M113 B08
RDD 00 (1)H
SH DTB H
DTB 09 M206 B09
0 TO DTB L
BMB 06 (1)H
DTB 06 M206 B09
BMB 03 (1)H
LPB TO DTB H
LPB 03 (1)H
M121 C08
DTB 03 M206 C09
BMB 00 (1)H
LPB 00 (1)H
DTB 00 M206 C09
SH EN H
-SH EN H
WB00 (0)H
M121 C10
+3V C15U1 H
WB00 M206 C14
BMB 10 (1)H
RDD 01 (1)H
DTB 10 M206 B09
BMB 07 (1)H
DTB 07 M206 B09
BMB 04 (1)H
LPB 04 (1)H
DTB 04 M206 C09
BMB 01 (1)H
LPB 01 (1)H
DTB 01 M206 C09
WB01 (0)H
WB01 M206 C14
BMB 11 (1)H
RDD 02 (1)H
DTB M206 B09
BMB 08 (1)H
DTB 08 M206 B09
BMB 05 (1)H
LPB 05 (1)H
DTB 05 M206 C09
BMB 02 (1)H
LPB 02 (1)H
DTB 02 M206 C09
WB02 (0)H
COMP + SH H
WB02 M206 C14
TC08-00001 A
D.SHEPARD 6/24/69
N.RHEAULT 6/24/69
D.LAZUKA 6/24/69 DTB/WB
D.LAZUKA 9/2/69
F.LASKEY 9/2/69
TC08
D BS TC08-0-8 A

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WR EN (Ø)H H2
C00 (Ø)H J2
M113 C15
K2
S2
M111 C13
T2 RD EN LPB 00-02 H

MKT (1)H L2
TP01 A H M2
M113 C15
N2
P2
M111 C17
R2
WRITE DATA H R2
ST FINAL (1)H S2
MK BLK END H T2
U2
M117 A09
V2
S2
M111 A11
T2 LPB TO DTB H

LPB 00 (Ø)L M1
LPB 01 (Ø)L N1
LPB 02 (Ø)L P1
LPB 03 (Ø)L R1
LPB 04 (Ø)L R2
LPB 05 (Ø)L S2
T2
U2
M119 D10
V2 LPB NOT EQ 1 H

WB00 (1)H A1
WR EN (1)H B1
RDD 00 (1)H C1
RD EN LPB 00-02 H D1
M121 D09
E1
D1 J 1 E1
B1 LPB 00 M207 D08
C1 K Ø F1
A1

DTB 00 (1)H D2
WR EN (1)H E2
RDD 00 (1)H F2
RD EN LPB 03-05 H H2
M121 D09
J2
F2 J 1 H2
D2 LPB 03 M207 D08
E2 K Ø J2

WR EN (Ø)H H2
TP01 H J2
M113 C11
K2
K2
L2
M2
N2
M627 D12
P2 < OR TO LPB H

WR EN (1)H D2
TP00 A H E2
C01 (Ø)H F2
M115 C12
H2

WB01 (1)H F1
WR EN (1)H H1
RDD 01 (1)H J1
RD EN LPB 00-02 H K1
M121 D09
L1
K1 J 1 L1
H1 LPB 01 M207 D08
J1 K Ø M1

DTB 01 (1)H K2
WR EN (1)H L2
RDD 01 (1)H M2
RD EN LPB 03-05 H N2
M121 D09
P2
N2 J 1 P2
L2 LPB 04 M207 D08
M2 K Ø R2
K2

MC02 (1)H D2
ST REV CK (1)H E2
F2
H2
M627 D12
J2 Ø TO LPB L

WB02 (1)H M1
WR EN (1)H N1
RDD 02 (1)H P1
RD EN LPB 00-02 H R1
M121 D09
S1
R1 J 1 S1
N1 LPB 02 M207 D08
P1 K Ø U1
Ø TO LPB L K2

DTB 02 (1)H R2
WR EN (1)H S2
RDD 02 (1)H T2
RD EN LPB 03-05 H U2
M121 D09
V2
U2 J 1 V2
S2 LPB 05 M207 D08
T2 K Ø V1
K2

WR EN (Ø)H D2
C00 (1)H E2
M113 C15
F2
P2
M111 C13
R2 RD EN LPB 03-05 H

RD EN LPB 00-02 H D2
XOR TO LPB H E2
F2
WREN (1)H H2
M121 C10
J2
M2
M111 C17
N2

RD EN 03-05 H R2
XOR TO LPB H S2
T2
WREN (1)H U2
M121 C10
V2
V1
M111 C17
U1

REVISIONS		
CHK	CHANGE NO.	REV.
NR	TC08-00001	A
	R.SU: KA 10-2-69	
	D.LAZUKA 10-6-69	
	TC08-00005	B

DRN. D.SHEPARD	DATE 5/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. N.RHEAULT	DATE 5/24/69	
ENG. D.LAZUKA	DATE 5/24/69	TITLE LPB
PROJ. ENG. D.LAZUKA	DATE 8/2/69	
PROD. F.LASKEY	DATE 8/2/69	
FIRST USED ON TC08		SIZE D CODE BS NUMBER TC08-0-9 REV. B
SCALE		
SHEET 1 OF 1		DIST.

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BAC Ø0 (1)L A1 M111 B06 B1 BAC Ø0 (1)H
BAC Ø1 (1)L D1 M111 B06 E1 BAC Ø1 (1)H
BAC Ø2 (1)L F1 M111 B06 H1 BAC Ø2 (1)H
BAC Ø3 (1)L J1 M111 B06 K1 BAC Ø3 (1)H
BAC Ø4 (1)L L1 M111 B06 M1 BAC Ø4 (1)H
BAC Ø5 (1)L N1 M111 B06 P1 BAC Ø5 (1)H
BAC Ø6 (1)L R1 M111 B06 S1 BAC Ø6 (1)H
BAC Ø7 (1)L V1 M111 B06 U1 BAC Ø7 (1)H
BAC Ø8 (1)L C1 M111 B06 D2 BAC Ø8 (1)H

BAC Ø9 (1)L E2 M111 B06 F2 BAC Ø9 (1)H
BAC 1Ø (1)L H2 M111 B06 J2 BAC 1Ø (1)H
BAC 11 (1)L K2 M111 B06 L2 BAC 11 (1)H
BMB Ø0 (1)L A1 M111 C06 B1 BMB Ø0 (1)H
BMB Ø1 (1)L D1 M111 C06 E1 BMB Ø1 (1)H
BMB Ø2 (1)L F1 M111 C06 H1 BMB Ø2 (1)H
BMB Ø3 (1)L J1 M111 C06 K1 BMB Ø3 (1)H
BMB Ø4 (1)L L1 M111 C06 M1 BMB Ø4 (1)H
BMB Ø5 (1)L N1 M111 C06 P1 BMB Ø5 (1)H

BMB Ø6 (1)L R1 M111 C06 S1 BMB Ø6 (1)H
BMB Ø7 (1)L V1 M111 C06 U1 BMB Ø7 (1)H
BMB Ø8 (1)L C1 M111 C06 D2 BMB Ø8 (1)H
BMB Ø9 (1)L E2 M111 C06 F2 BMB Ø9 (1)H
BMB 1Ø (1)L H2 M111 C06 J2 BMB 1Ø (1)H
BMB 11 (1)L K2 M111 C06 L2 BMB 11 (1)H

G821 A01: S1 +5 SENSE, N2 GND SENSE, A2, B1, C1, D1, E1, F1, H1, J1, K1, L1 +5V, M1, N1, P1, R1, C2, D2, H2 GND, J2, K2 GND, L2, T1 GND

G821 B01: S1, N2, A2 +5V, B1, C1, D1, E1, F1, H1, J1, K1, L1, M1, N1, P1, R1, C2 GND, D2, H2, J2, K2, L2, T1 GND

CKØØ (1)L, TM EN H, CKØØ (1)H → G888 A18 → T TRK (1)H, T TRK (1)L

WBØØ (1)H, TM EN H, WBØØ (1)L → G888 B18 → RDMK (1)H, RDMK (1)L

WBØ2 (1)H, WR EN (1)H, WBØ2 (1)L → G888 A20 → RDD 22 (1)H, RDD Ø2 (1)L

WBØ1 (1)H, WR EN (1)H, WBØ1 (1)L → G888 B20 → RDD Ø1 (1)H, RDD Ø1 (1)L

WBØØ (1)H, WR EN (1)H, WBØØ (1)L → G888 A21 → RDD Ø0 (1)H, RDD Ø0 (1)L

W032 A19 and W032 B19 connectors

REVISIONS		
CHK	CHANGE NO.	REV.
	TC08-00005	A

DRN. D.SHEPARD	DATE 6/24/68	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D N.RHEAULT	DATE 6/24/68	
ENG. J.LAZUKA	DATE 6/24/68	TITLE I/O BIS INVTS READ WRITE AMPS
PROJ. ENG. J.LAZUKA	DATE 9/2/69	
PROD. F.LASKEY	DATE 9/2/69	
FIRST USED ON TC08		SIZE D, CODE 8S, NUMBER TC08-0-10, REV. A
SCALE		
SHEET 1 OF 1		DIST.

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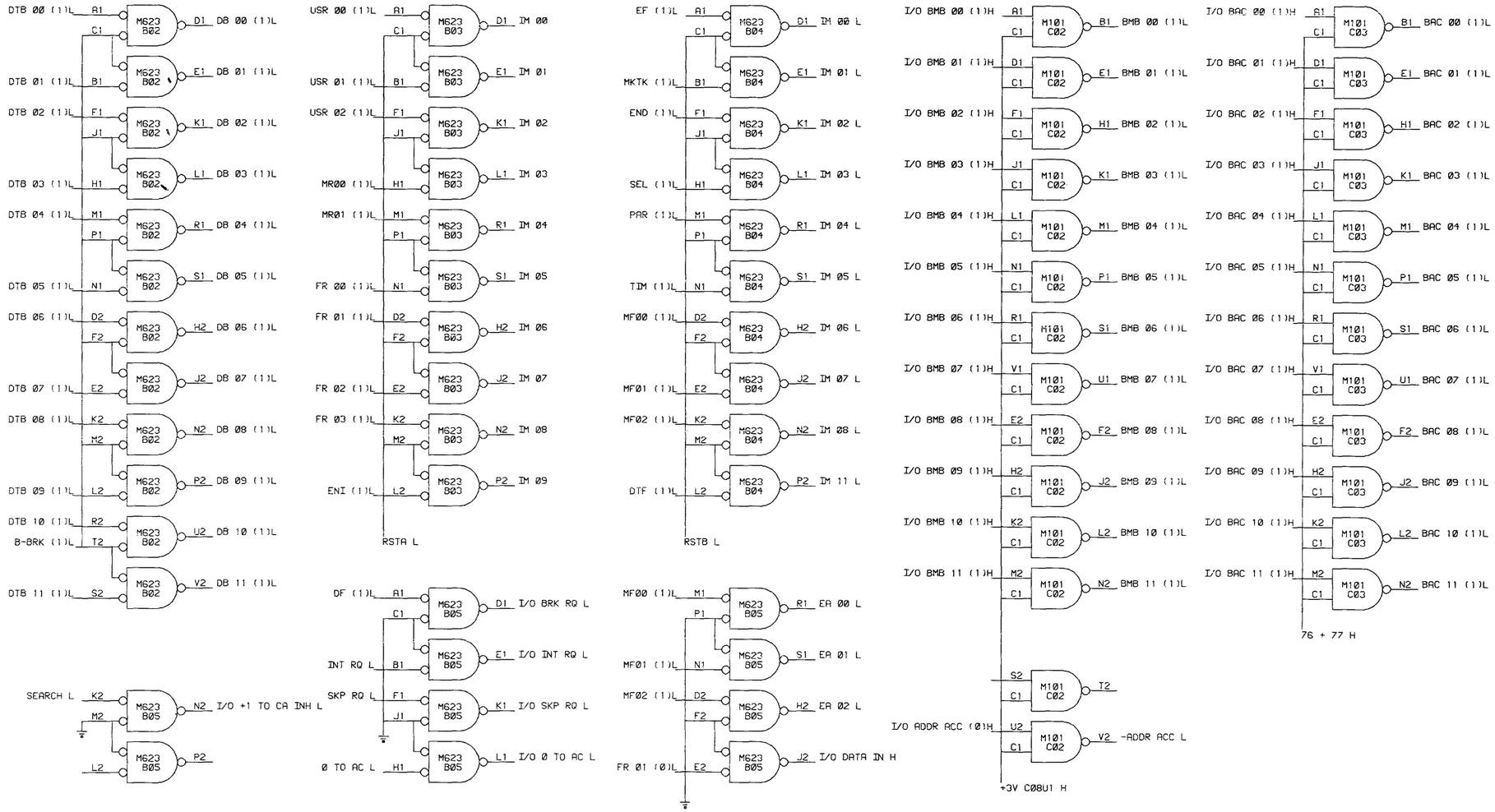

REVISIONS		
CHK	CHANGE NO.	REV.
NR	TC08-00001	A
	R SOPKA 10-2-69	
	D LAZUKA	
	TC08-00024	B

DRN. D.SHEPARD	DATE 5/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. N.RHEAULT	DATE 5/24/69	
ENG. D.LAZUKA	DATE 5/24/69	TITLE I/O BUS DRIVE/RECIEVE
PROJ. ENG. D.LAZUKA	DATE 9/2/69	
PROD. F.LASKEY	DATE 9/2/69	
FIRST USED ON TC08		
SCALE		SIZE D, CODE BS, NUMBER TC08-0-11, REV. B
SHEET 1 OF 1		DIST.

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M903 A02
A1 B1 I/O BAC 00 (1)H
C1
D1 I/O BAC 01 (1)H
E1 I/O BAC 02 (1)H
F1
H1 I/O BAC 03 (1)H
J1 I/O BAC 04 (1)H
K1
L1 I/O BAC 05 (1)H
M1 I/O BAC 06 (1)H
N1
P1 I/O BAC 07 (1)H
R1
S1 I/O BAC 08 (1)H
T1
U1
V1

M903 A03
A1 B1 IO BMB 00 (1)H
C1
D1 I/O BMB 01 (1)H
E1 I/O BMB 02 (1)H
F1
H1 I/O BMB 03 (0)H
J1 I/O BMB 03 (1)H
K1
L1 I/O BMB 04 (0)H
M1 I/O BMB 04 (1)H
N1
P1 I/O BMB 05 (0)H
R1
S1 I/O BMB 05 (1)H
T1
U1
V1

M903 A04
A1 B1 IM 00 L
C1
D1 IM 01 L
E1 IM 02 L
F1
H1 IM 03 L
J1 IM 04 L
K1
L1 IM 05 L
M1 IM 06 L
N1
P1 IM 07 L
R1
S1 IM 08 L
T1
U1
V1

M903 A05
A1 B1 C1 D1 E1 F1 H1 J1 K1 L1 M1 N1 P1 R1 S1 T1 U1 V1

M903 A06
A1 B1 DB 00 (1)L
C1
D1 DB 01 (1)L
E1 DB 02 (1)L
F1
H1 DB 03 (1)L
J1 DB 04 (1)L
K1
L1 DB 05 (1)L
M1 DB 06 (1)L
N1
P1 DB 07 (1)L
R1
S1 DB 08 (1)L
T1
U1
V1

M903 A02
A2 B2 C2
D2 I/O BAC 09 (1)H
E2 I/O BAC 10 (1)H
F2
H2 I/O BAC 11 (1)H
J2
K2 IOP 1 H
L2
M2 IOP 2 H
N2
P2 IOP 4 H
R2
S2 I/O TS03 H
T2 I/O TS04 H
U2
V2 I/O PWR CLR H

M903 A03
A2 B2 C2
D2 I/O BMB 06 (0)H
E2 I/O BMB 06 (1)H
F2
H2 I/O BMB 07 (0)H
J2
K2 I/O BMB 07 (1)H
L2
M2 I/O BMB 08 (0)H
N2
P2 I/O BMB 08 (1)H
R2
S2 I/O BMB 09 (1)H
T2 I/O BMB 10 (1)H
U2
V2 I/O BMB 11 (1)H

M903 A04
A2 B2 C2
D2 IM 09 L
E2 IM 10 L
F2
H2 IM 11 L
J2
K2 I/O SKP RQ L
L2
M2 I/O INT RQ L
N2
P2 I/O Ø TO AC L
R2
S2 I/O B-RUN (Ø)L
T2
U2
V2

M903 A05
A2 B2 C2 D2 E2 F2 H2 J2
K2 I/O BRK RQ L
L2
M2 I/O DATA IN H
N2
P2 I/O B-BRK (Ø)L
R2
S2 I/O ADDR ACC (Ø)H
T2
U2
V2

M903 A06
A2 B2 C2
D2 DB 09 (1)L
E2 DB 10 (1)L
F2
H2 DB 11 (1)L
J2
K2
L2
M2 I/O +1 TO CA INH L
N2
P2 I/O BWCO L
R2
S2 EA 02 L
T2 EA 01 L
U2
V2 EA 00 L

M903 D02
A1 B1 I/O BAC 00 (1)H
C1
D1 I/O BAC 01 (1)H
E1 I/O BAC 02 (1)H
F1
H1 I/O BAC 03 (1)H
J1 I/O BAC 04 (1)H
K1
L1 I/O BAC 05 (1)H
M1 I/O BAC 06 (1)H
N1
P1 I/O BAC 07 (1)H
R1
S1 I/O BAC 08 (1)H
T1
U1
V1

M903 D03
A1 B1 I/O BMB 00 (1)H
C1
D1 I/O BMB 01 (1)H
E1 I/O BMB 02 (1)H
F1
H1 I/O BMB 03 (0)H
J1 I/O BMB 03 (1)H
K1
L1 I/O BMB 04 (0)H
M1 I/O BMB 04 (1)H
N1
P1 I/O BMB 05 (0)H
R1
S1 I/O BMB 05 (1)H
T1
U1
V1

M903 D04
A1 B1 IM 00 L
C1
D1 IM 01 L
E1 IM 02 L
F1
H1 IM 03 L
J1 IM 04 L
K1
L1 IM 05 L
M1 IM 06 L
N1
P1 IM 07 L
R1
S1 IM 08 L
T1
U1
V1

M903 D05
A1 B1 C1 D1 E1 F1 H1 J1 K1 L1 M1 N1 P1 R1 S1 T1 U1 V1

M903 D06
A1 B1 DB 00 (1)L
C1
D1 DB 01 (1)L
E1 DB 02 (1)L
F1
H1 DB 03 (1)L
J1 DB 04 (1)L
K1
L1 DB 05 (1)L
M1 DB 06 (1)L
N1
P1 DB 07 (1)L
R1
S1 DB 08 (1)L
T1
U1
V1

M903 D02
A2 B2 C2
D2 I/O BAC 09 (1)H
E2 I/O BAC 10 (1)H
F2
H2 I/O BAC 11 (1)H
J2
K2 IOP 1 H
L2
M2 IOP 2 H
N2
P2 IOP 4 H
R2
S2 I/O TS03 H
T2 I/O TS04 H
U2
V2 I/O PWR CLR H

M903 D03
A2 B2 C2
D2 I/O BMB 06 (0)H
E2 I/O BMB 06 (1)H
F2
H2 I/O BMB 07 (0)H
J2
K2 I/O BMB 07 (1)H
L2
M2 I/O BMB 08 (0)H
N2
P2 I/O BMB 08 (1)H
R2
S2 I/O BMB 09 (1)H
T2 I/O BMB 10 (1)H
U2
V2 I/O BMB 11 (1)H

M903 D04
A2 B2 C2
D2 IM 09 L
E2 IM 10 L
F2
H2 IM 11 L
J2
K2 I/O SKP RQ L
L2
M2 I/O INT RQ L
N2
P2 I/O Ø TO AC L
R2
S2 I/O B-RUN (Ø)L
T2
U2
V2

M903 D05
A2 B2 C2 D2 E2 F2 H2 J2
K2 I/O BRK RQ L
L2
M2 I/O DATA IN H
N2
P2 I/O B-BRK (Ø)L
R2
S2 I/O ADDR ACC (Ø)H
T2
U2
V2

M903 D06
A2 B2 C2
D2 DB 09 (1)L
E2 DB 10 (1)L
F2
H2 DB 11 (1)L
J2
K2
L2
M2 I/O +1 TO CA INH L
N2
P2 I/O BWCO L
R2
S2 EA 02 L
T2 EA 01 L
U2
V2 EA 00 L

W023 A24
A2 B2
C2 T GO L
D2 T STOP L
E2 T FWD L
F2 T REV L
H2 T PWR CLR L
J2
K2 T SINGLE UNIT L
L2 T WRITE OK L
M2 T Ø1 L
N2 T Ø2 L
P2 T Ø3 L
R2 T Ø4 L
S2 T Ø5 L
T2 T Ø6 L
U2 T Ø7 L
V2 T Ø0 L

M916 A25
A1 USR Ø0 (1)H
B1 USR Ø1 (1)H
C1 USR Ø2 (1)H
D1 MR0Ø (1)H
E1 MR01 (1)H
F1 FR Ø0 (1)H
H1 FR Ø1 (1)H
J1 FR Ø2 (1)H
K1 FR Ø3 (1)H
L1 ENI (1)H
M1
N1 EF (1)H
P1 MKTK (1)H
R1 END (1)H
S1 SEL (1)H
T1 PAR (1)H
U1 TIM (1)H
V1 MF00 (1)H

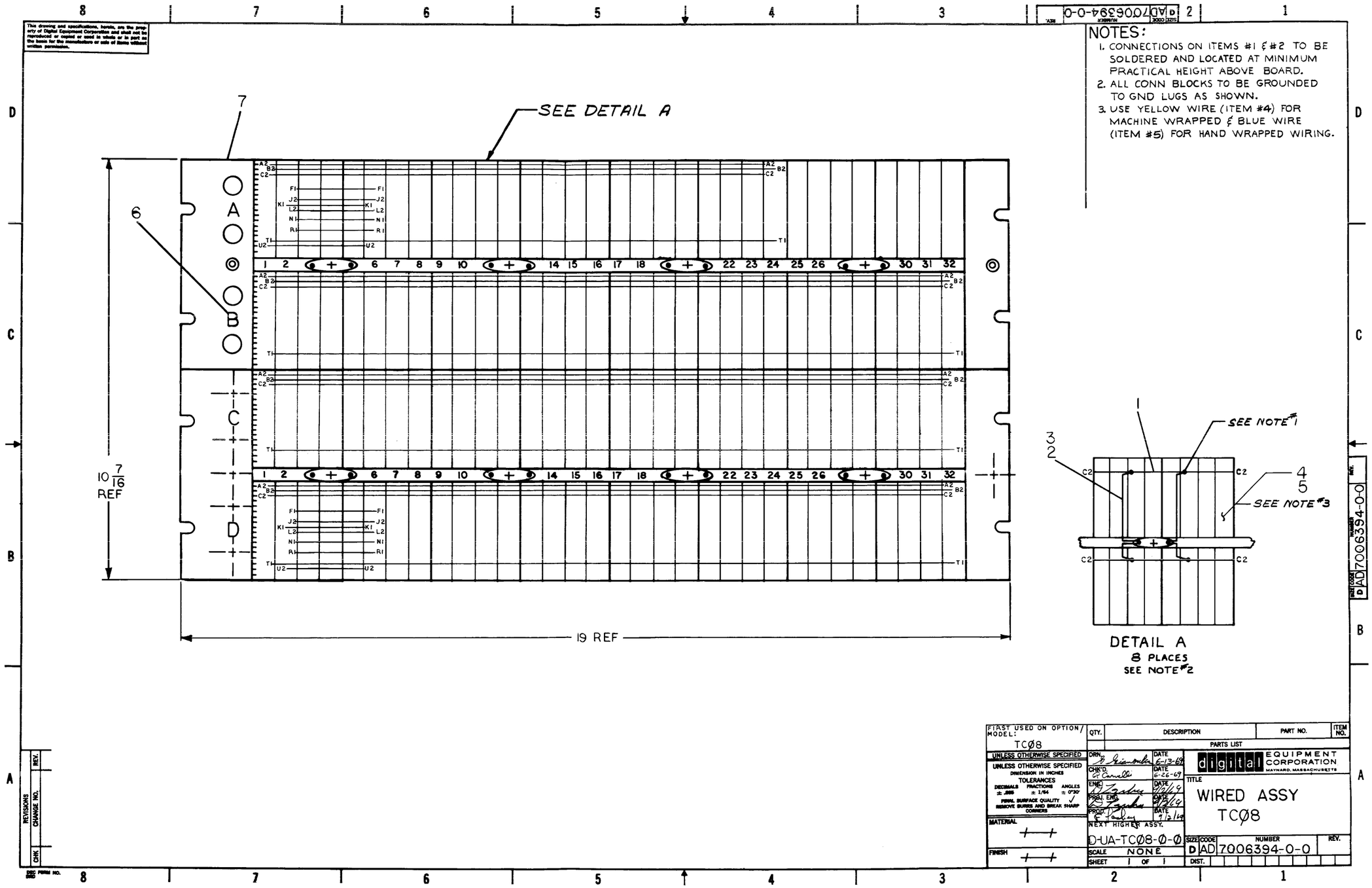
M916 A25
A2 DTB Ø0 (1)H
B2 DTB Ø1 (1)H
C2 DTB Ø2 (1)H
D2 DTB Ø3 (1)H
E2 DTB Ø4 (1)H
F2 DTB Ø5 (1)H
H2 DTB Ø6 (1)H
J2 DTB Ø7 (1)H
K2 DTB Ø8 (1)H
L2 DTB Ø9 (1)H
M2 DTB 10 (1)H
N2 DTB 11 (1)H
P2 WB00 (1)H
R2 WB01 (1)H
S2 WB02 (1)H
T2 LPB 00 (1)H
U2 LPB Ø1 (1)H
V2 LPB Ø2 (1)H

M916 A26
A1 MF01 (1)H
B1 MF02 (1)H
C1 DTF (1)H
D1
E1 DF (1)H
F1 WR EN (1)H
H1 WC (1)H
J1 UTS (1)H
K1 ST BLK MK (1)H
L1 ST REV CK (1)H
M1 DATA (1)H
N1 ST FINAL (1)H
P1 ST CK (1)H
R1 ST IDLE (1)H
S1 MC00 (1)H
T1 MC01 (1)H
U1 MC02 (1)H
V1

M916 A26
A2 LPB Ø3 (1)H
B2 LPB Ø4 (1)H
C2 LPB Ø5 (1)H
D2
E2 C00 (1)H
F2 C01 (1)H
H2 MKT (1)H
J2 W01 (1)H
K2 W02 (1)H
L2 W03 (1)H
M2 W04 (1)H
N2 W05 (1)H
P2 W06 (1)H
R2 W07 (1)H
S2 W08 (1)H
T2 W09 (1)H
U2
V2 SWTM H

CHK	CHANGE NO.	REV.
NR	TC08-00001	A
R SOFKA 10-2-69		
D LAZUKA		
28-00004		B

DRN. D.SHEPARD	DATE 6/24/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. N.RHEAULT	DATE 6/24/69	
ENG. D.LAZUKA	DATE 6/24/69	TITLE I/O BUS+CONNECTORS
PROJ. ENG. D.LAZUKA	DATE 6/2/69	
PROD. F.LASKEY	DATE 6/2/69	
FIRST USED ON TC08		SIZE D CODE IC NUMBER TC08-0-12 REV. B
SCALE		
SHEET 1 OF 1		DIST.



NOTES:

1. CONNECTIONS ON ITEMS #1 & #2 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BOARD.
2. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
3. USE YELLOW WIRE (ITEM #4) FOR MACHINE WRAPPED & BLUE WIRE (ITEM #5) FOR HAND WRAPPED WIRING.

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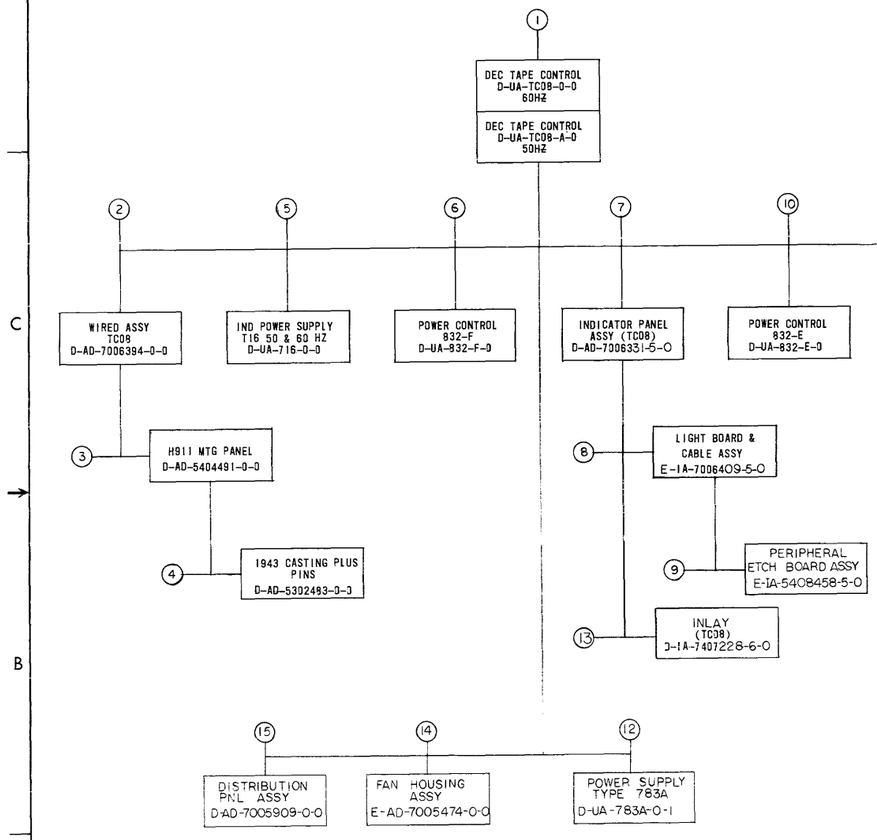

MECHANICAL

FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F C
1.	DEC TAPE CONTROL	D-UA-TC08-0-0			
	DEC TAPE CONTROL	D-UA-TC08-A-0			
	DEC TAPE CONTROL (PL)	A-PL-TC08-0-0			
	CABLE, DUAL MYLAR M903-(2) W031	D-UA-BC08C-0-0			
2.	WIRED ASSY TC08	D-AD-7006394-0-0			
	WIRED ASSY TC08 (PL)	A-PL-7006394-0-0			
	LOGIC FRAME DECALS	A-DC-7406371-0-0			
3.	H911 MTG PANEL	D-AD-5404491-0-0			
	H911 MTG PANEL (PL)	A-PL-5404491-0-0			
4.	1943 CASTING PLUS PINS	D-AD-5302483-0-0			
	1943 CASTING PLUS PINS (PL)	A-PL-5302483-0-0			
	1943 FRAME CASTING	E-MD-1202885-0-0			
5.	IND POWER SUPPLY 716	D-UA-716-0-0			
	IND POWER SUPPLY 716 (PL)	A-PL-716-0-0			
6.	POWER CONTROL 832-F	D-UA-832-F-0			
	POWER CONTROL 832-F (PL)	A-PL-832-F-0			
7.	INDICATOR PANEL ASSY (TC08)	D-AD-7006331-5-0			
	INDICAIOR PANEL ASSY (TC08) (PL)	C-PL-7006331-5-0			
8.	LIGHT BOARD & CABLE ASSY	E-IA-7006409-5-0			
9.	PERIPHERAL ETCH BOARD ASSY	E-IA-5408458-5-0			
10.	POWER CONTROL 832-E	D-UA-832-E-0			
	POWER CONTROL 932-E (PL)	A-PL-832-E-0			
11.	783 POWER SUPPLY	D-UA-783-0-1			
	783 POWER SUPPLY (PL)	A-PL-783-0-1			
12.	POWER SUPPLY TYPE 783A	D-UA-783A-0-1			
	POWER SUPPLY TYPE 783A (PL)	A-PL-783A-0-1			
13.	INDICATOR PANEL (TC08)	E-IA-7407228 5 0			
	IND PANEL SILK SCREEN	C-SS-7407228-0-6			
	IND PANEL SILK SCREEN	C-SS-7407228-G-2			
14.	FAN HOUSING ASSY	E-AD-7005474-0-0			
	FAN HOUSING ASSY (PL)	A-PL-7005474-0-0			
15.	DISTRIBUTION PANEL ASSY	D-AD-7005909-0-0			
	DIST PANEL ASSY (PL)	A-PL-7005909-0-0			

ELECTRICAL

FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F C
1.	DEC TAPE CONT	A-ML-TC08-0			
	DEC TAPE CONT	A-ML-TC08-A			
	I/O CONTROL	D-BS-TC08-0-1			
	STATUS 'A'	D-BS-TC08-0-2			
	TP GEN	D-BS-TC08-0-3			
	FLAGS	D-BS-TC08-0-4			
	CONTROL	D-BS-TC08-0-5			
	ERRORS	D-BS-TC08-0-6			
	MARK TRACK DECODE	D-BS-TC08-0-7			
	DTB/WB	D-BS-TC08-0-8			
	LPB	D-BS-TC08-0-9			
	I/O BIS INVTS-IND DVRS	D-BS-TC08-0-10			
	I/O BUS DRIVE RECEIVE	D-BS-TC08-0-11			
	I/O BUS CONNECTORS	D-BS-TC08-0-12			
	MODULE UTILIZATION LIST	K-MU-TC08-0-13			
	MODULE UTILIZATION LIST	K-PL-TC08-0-13			
	WIRE LIST TC08	K-WL-TC08-0-14			
	CHECKOUT PROCEDURE	A-SP-TC08-0-16			
	TIMING DIAGRAM	D-TD-TC08-0-17			
2.	WIRED ASSY TC08	D-AD-7006394-0-0			
	WIRED ASSY TC08 (PL)	A-PL-7006394-0-0			

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: TC08

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

		DATE
DRN.	D Marum	6/3/69
CHK'D	Clark	7/16/69
ENG.	Gula	7/16/69
PROJ. ENG.		
PROD.		

NEXT HIGHER ASSY: A-ML-TC08-0

SCALE —

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: DECTAPE CONTROL

SIZE	CODE	NUMBER	REV.
D	DI	TC08-0-15	B

DIST.

REVISIONS	REV.	CHK	
CHANGE NO. TC08-00002	A	D.LAZUKA	11/20/68
TC08-00003	B	D.LAZUKA	7/1/70

DEC FORM NO DRD 100

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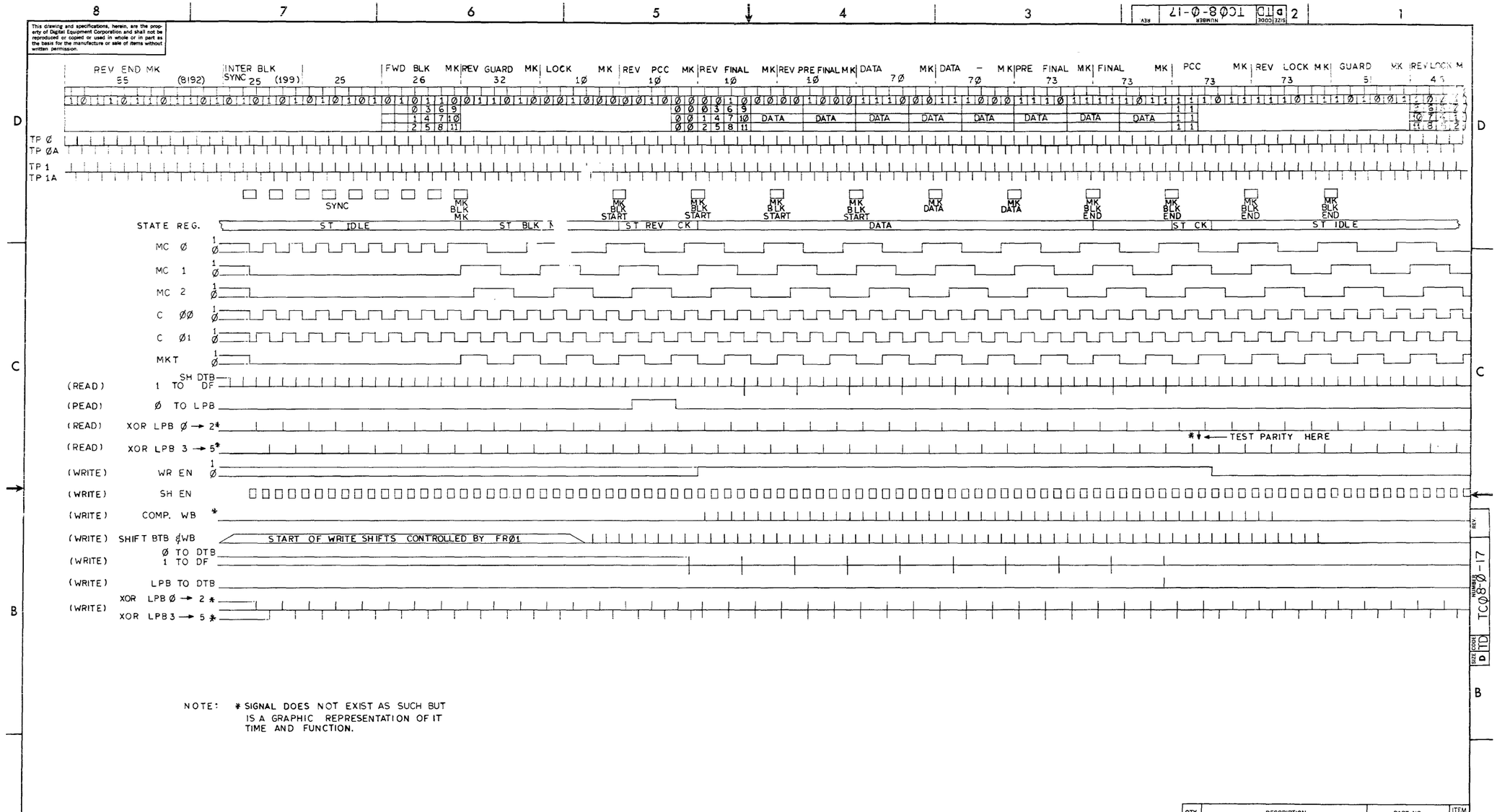


NOTE: * SIGNAL DOES NOT EXIST AS SUCH BUT IS A GRAPHIC REPRESENTATION OF IT TIME AND FUNCTION.

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
= .005 = 1/64 = 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.		DATE 10/6/69
CHK'D.		DATE 10/9/69
ENG.		DATE 10/9/69
PROJ. ENG.		DATE 10/9/69
PROD. ENG.		DATE 10/6/69

FIRST USED ON

SCALE

SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE
TCØ8 TIMING

SIZE	CODE	NUMBER	REV.
D	TD	TCØ8-Ø-17	

DIST.

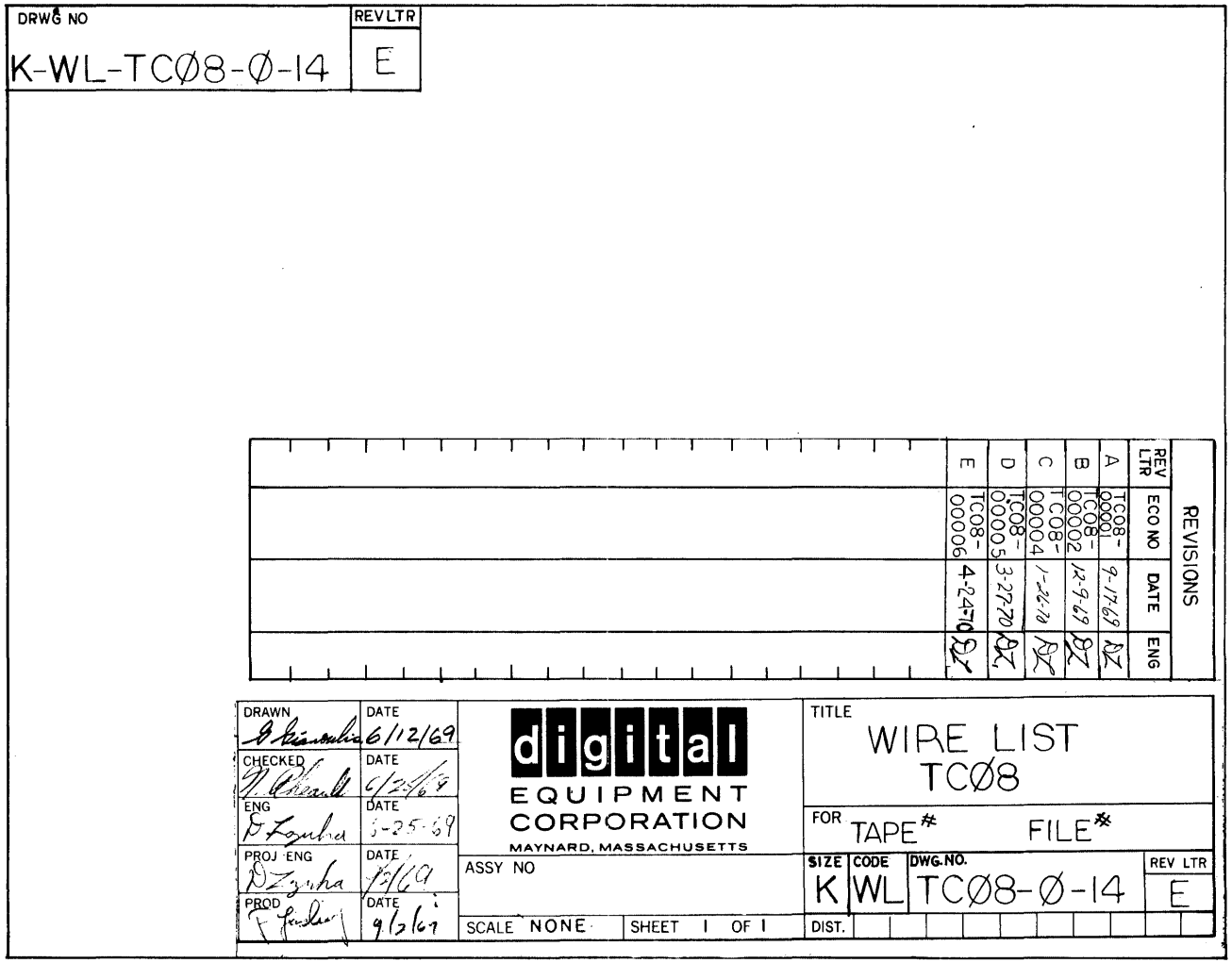
REVISIONS	REV.	CHANGE NO	CHK

DEC FORM NO DRD 102A

DWG NO	REV
MU K-PL-TC08-0-13	C

REVISIONS		
CHK	CHANGE NO.	REV.
[illegible]	TC08-00002	A
[illegible]	D. LAZUKA	
[illegible]	TC08-00004	B
[illegible]	D. LAZUKA	
FV	TC08-00006	C
	T. Quillin 4-24-70	
	LAZUKA	
	[illegible] 4-24-70	

DRN. Donna Shepard	DATE 6-24-69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. [illegible]	DATE 6-24-69	TITLE MODULE UTILIZATION+ PARTS LIST
ENG. [illegible]	DATE 6-24-69	
PROJ. ENG. [illegible]	DATE	
PROD. [illegible]	DATE 9/2/69	
FIRST USED ON		
SCALE NONE		SIZE K · CODE MU PL · NUMBER TC08-0-13 · REV. C
SHEET OF 8		


DRWG NO
K-WL-TCØ8-Ø-14
REV LTR
E
REVISIONS
REV LTR
ECO NO
DATE
ENG
A TC08-00001 9-17-69 DZ
B TC08-00002 12-9-69 DZ
C TC08-00004 1-26-70 DZ
D TC08-00005 3-27-70 DZ
E TC08-00006 4-24-70 DZ
DRAWN
DATE 6/12/69
CHECKED
DATE 6/24/69
ENG
DATE 5-25-69
PROJ ENG
DATE 7/1/69
PROD
DATE 9/2/69
digital
EQUIPMENT
CORPORATION
MAYNARD, MASSACHUSETTS
ASSY NO
SCALE NONE
SHEET 1 OF 1
TITLE
WIRE LIST
TCØ8
FOR TAPE* FILE*
SIZE K
CODE WL
DWG. NO. TCØ8-Ø-14
REV LTR E
DIST.

Digital Equipment Corporation
Maynard, Massachusetts

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